ECE 205 “Electrical and Electronics Circuits”

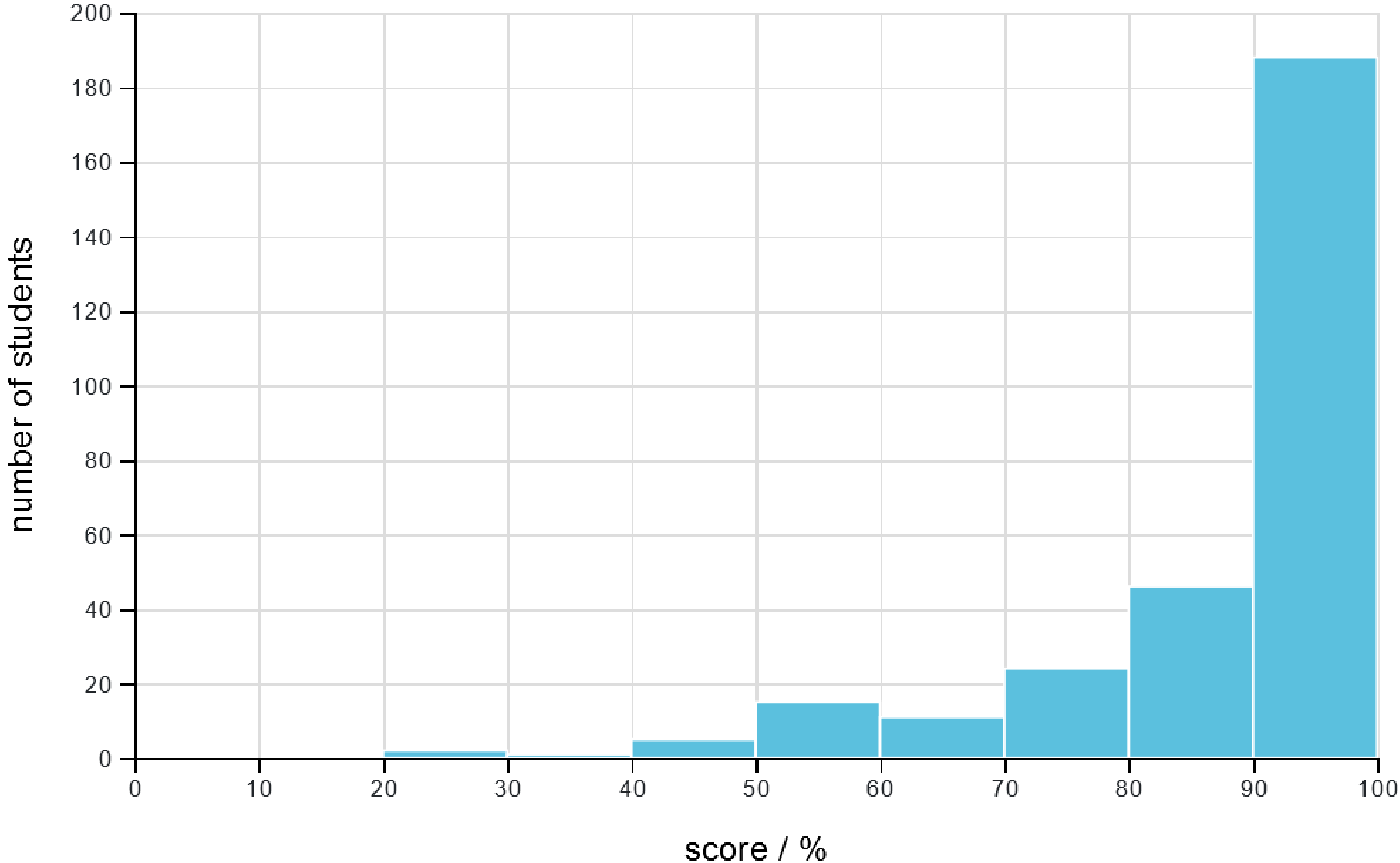
Spring 2022 – LECTURE 29

MWF – 12:00pm

Prof. Umberto Ravaioli

2062 ECE Building

Quiz 3 – Score Distribution



Quiz 3 – Statistics

Number of students	292
Mean score	88%
Standard deviation	14%
Median score	95%
Minimum score	28%
Maximum score	100%
Number of 0%	0 (0% of class)
Number of 100%	28 (10% of class)

Lecture 29 – Summary

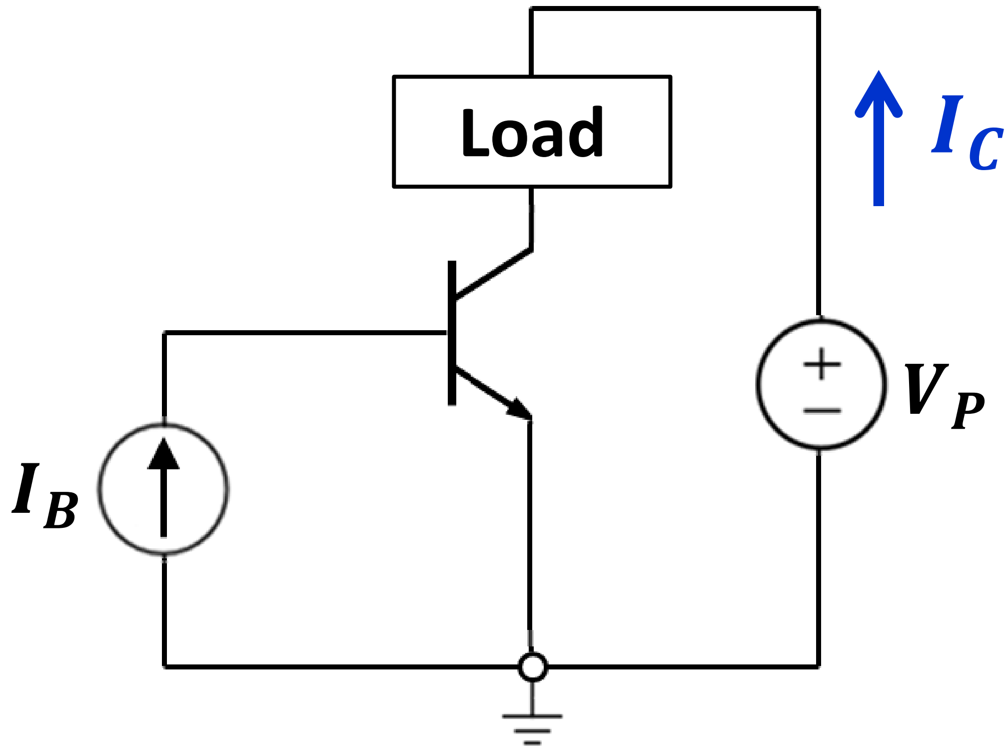
Learning Objectives

1. Power in Transistors
2. Binary logic
3. Elementary logic operators
4. Boolean algebra

Power in Transistors

BJT as a switch

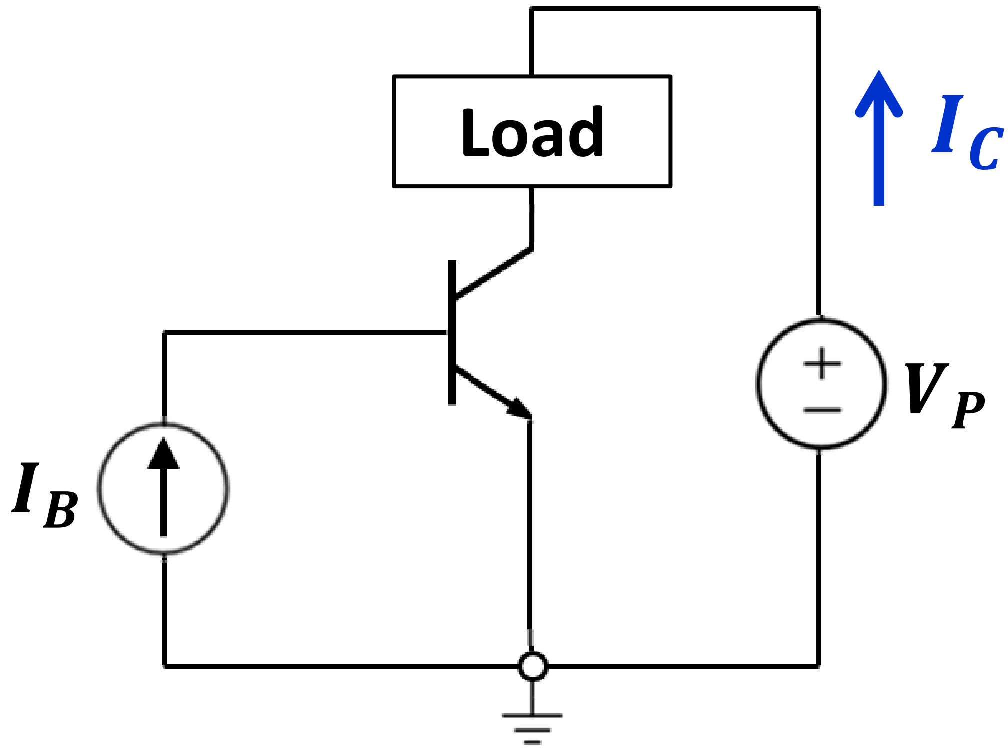
The BJT has important applications as a current controlled "valve" or as a "logic" element



We wish to switch ON and OFF power consumption by the load using a BJT instead of a mechanical switch.

BJT as a switch

Power consumed by the transistor is lost (it is part of operations costs)



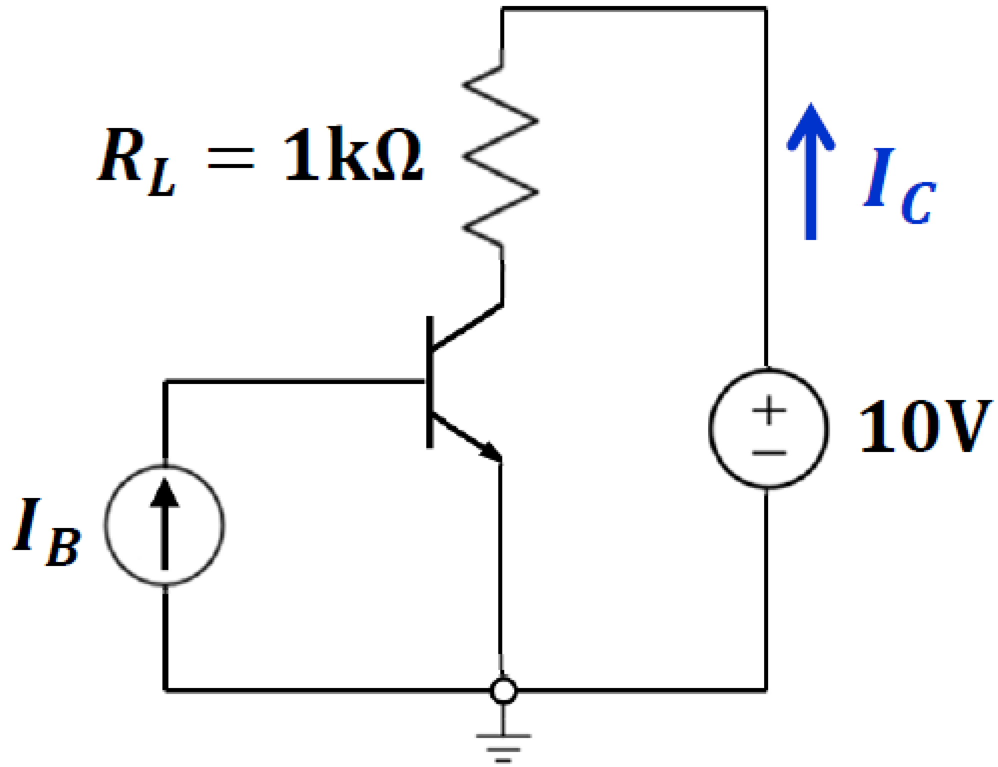
$$P_{BJT} = V_{BE} \times I_B + V_{CE} \times I_C$$

Example: Find P_{BJT} and P_{Load}

$V_{BE}(\text{on}) = 0.7\text{V}$

$V_{CE}(\text{sat}) = 0.2\text{V}$

$\beta = 50$



1. $I_B = 0\ \text{mA}$
2. $I_B = 0.1\ \text{mA}$
3. $I_B = 0.5\ \text{mA}$

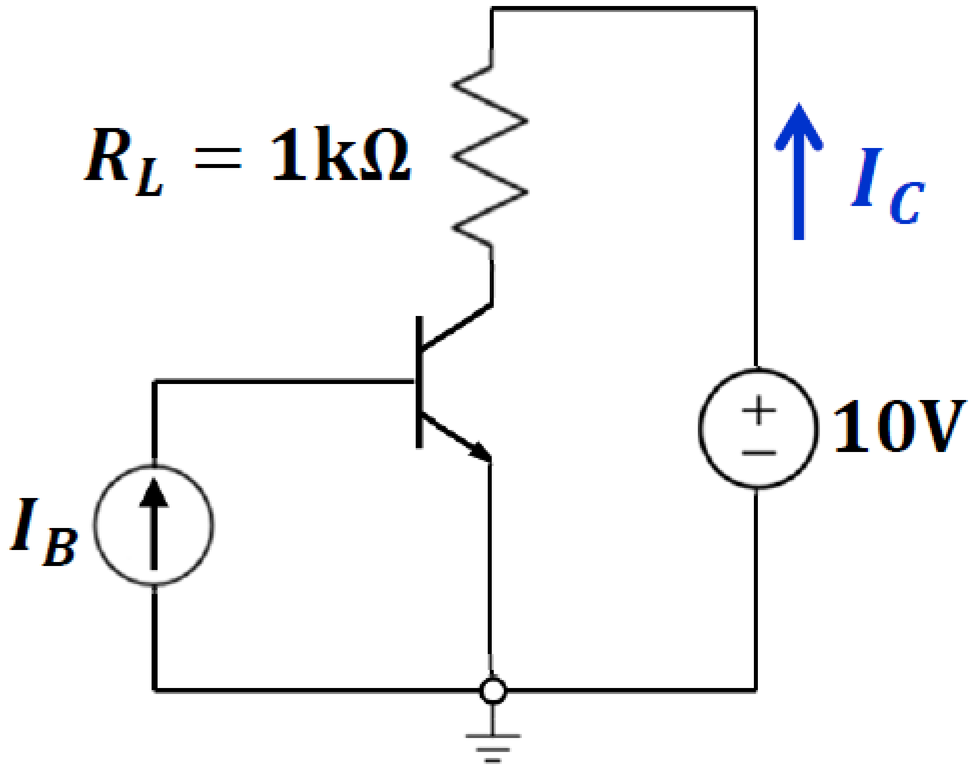
Example: Find P_{BJT} and P_{Load}

$V_{BE}(\text{on}) = 0.7\text{V}$

$V_{CE}(\text{sat}) = 0.2\text{V}$

$\beta = 50$

1. $I_B = 0 \text{ mA}$



BJT is OFF

$$P_{BJT} = 0 \text{ W}$$

$$P_{Load} = 0 \text{ W}$$

This is the state in which the transistor switch is OPEN and the load is idle. In reality, there will be some current leakage in the non-ideal p-n junctions consuming minute amount of power, but this is negligible in circuits with a small number of transistors.

Now we CLOSE the switch, to let current flow through the load R_L.

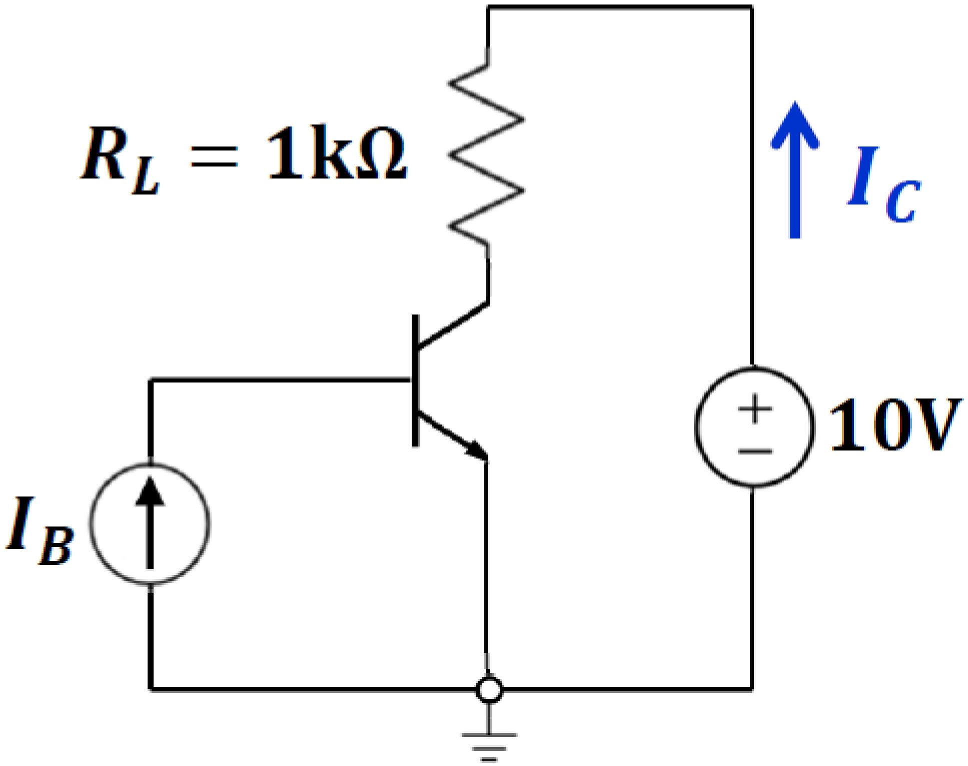
Which state of operation should we prefer for the BJT to be ON, in order to minimize the power consumed by the switch itself?

Example: Find P_{BJT} and P_{Load}

$V_{BE}(\text{on}) = 0.7\text{V}$

$V_{CE}(\text{sat}) = 0.2\text{V}$

$\beta = 50$



2. $I_B = 0.1\ \text{mA}$

Assume Forward Active mode

$I_C = \beta I_B = 5\text{mA}$

$V_{CE} = 10 - I_C R_L = 5\text{V}$

$P_{BJT} = V_{BE} \times I_B + V_{CE} \times I_C = 0.7 \times 0.1\,\text{m} + 5 \times 5\,\text{m}$

$P_{BJT} = 25.07\text{mW}$

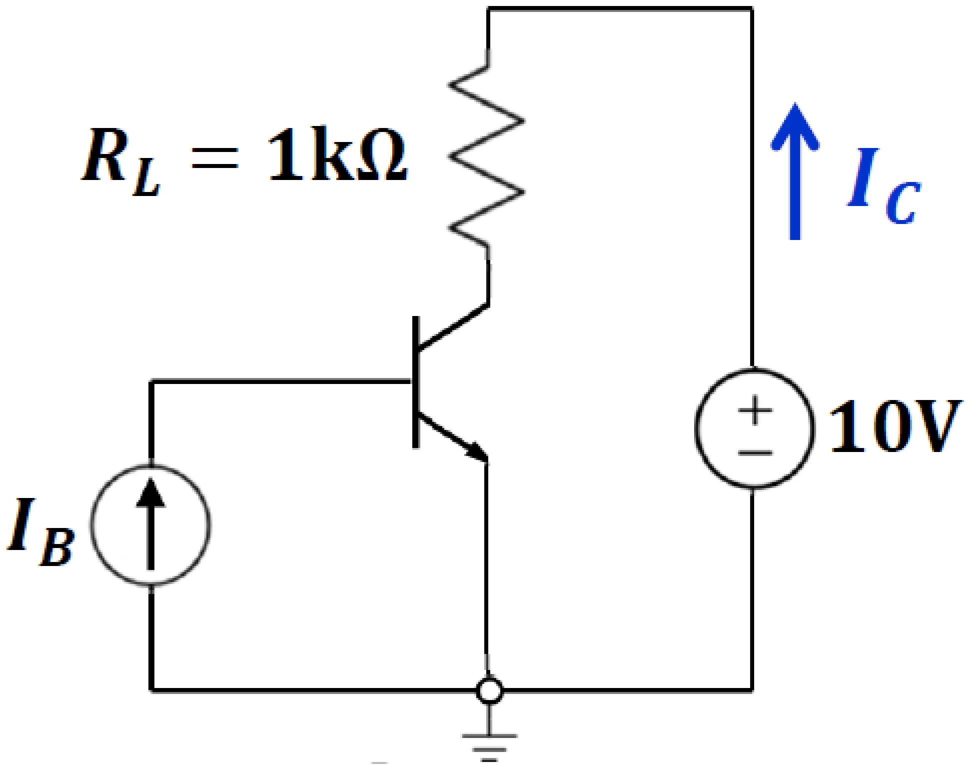
$P_{Load} = I_C^2 R_L = (5\text{mA})^2 \times 1\text{k}\Omega = 25\text{mW}$

Example: Find P_{BJT} and P_{Load}

$V_{BE}(\text{on}) = 0.7\text{V}$

$V_{CE}(\text{sat}) = 0.2\text{V}$

$\beta = 50$



3. $I_B = 0.5\text{ mA}$

BJT is in Saturation

$I_C(\text{sat}) = 9.8\text{mA}$

$$P_{BJT} = 0.7 \times 0.5\text{m} + 0.2 \times 9.8\text{m} = 2.31\text{ mW}$$

$$P_{Load} = I_C^2 R_L = (9.8\text{mA})^2 \times 1\text{k}\Omega = 96.04\text{mW}$$

BJT is most efficient as a switch in Saturation

Introduction to Digital Logic

Binary Computer Logic

Logic is a science which studies the reasoning needed to reach a conclusion or make a decision.

Computer operations are based on a form of logic which considers two possible states: TRUE or FALSE.

In a computer, these states are encoded into numbers.

For instance:

FALSE = 0

TRUE = 1

Binary Number System

The total number of digits, used to express numbers, is called the "base". We normally use the base-10 (or decimal) number system, with digits from 0 to 9.

Similarly, the complete number system can be constructed with a base of two numbers: 0 and 1. This is the base-2 or "binary" system.

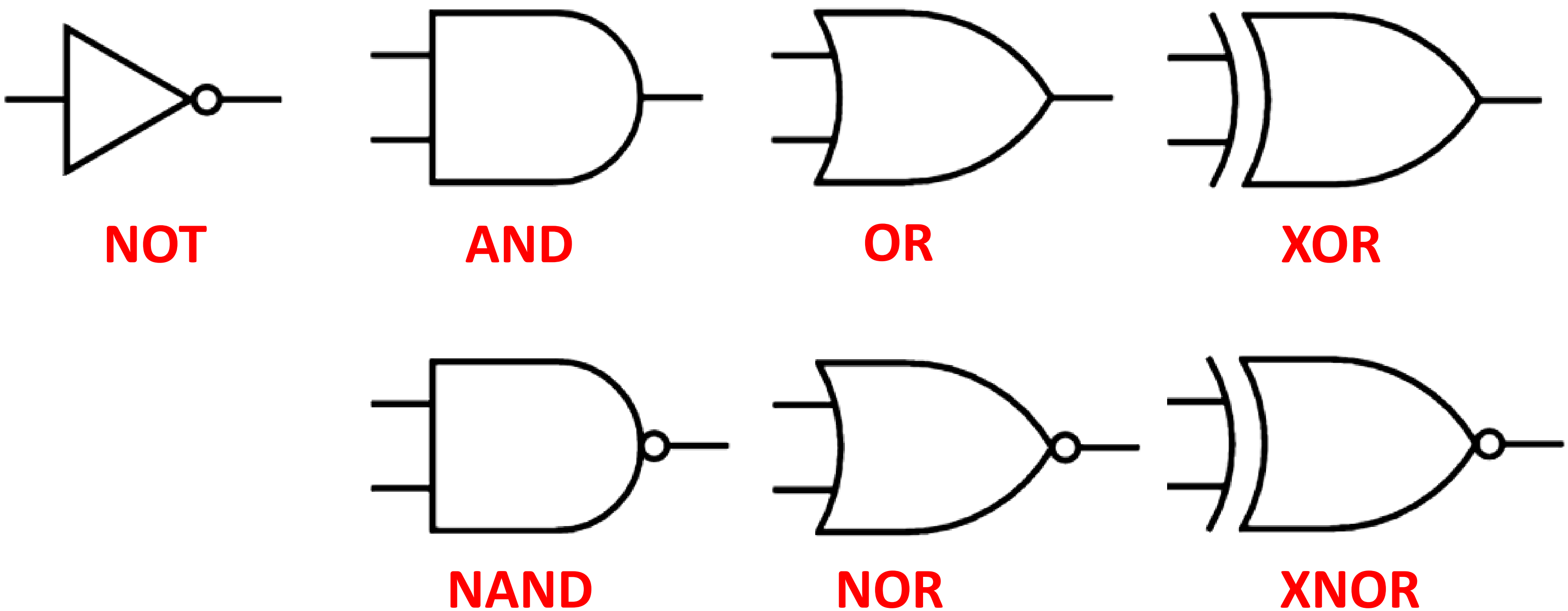
Examples:

DECIMAL	BINARY
5	101
13	1101
24	11000
100	1100100

64 32 4

Logic Operations

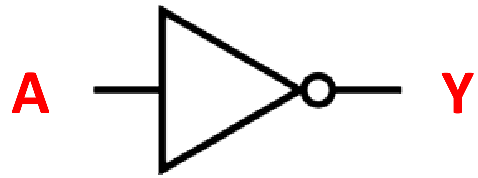
Binary logic is based on a set of seven elementary logical operations with two inputs and one output. The elements which accomplish these operations are called “Logic Gates”. They are represented with the symbols below in a logic circuit.



INPUT OUTPUT TRUTH TABLE

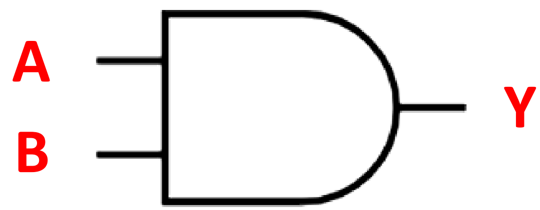
NOT

(inverter)



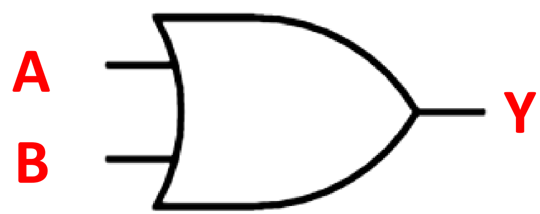
A	Y
0	1
1	0

AND



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

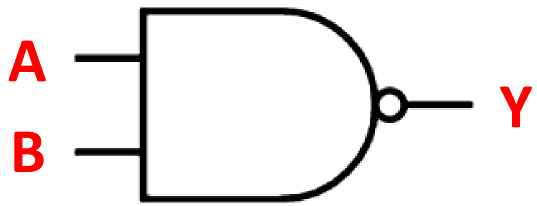
OR



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

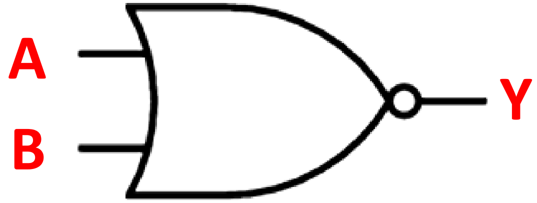
INPUT OUTPUT TRUTH TABLE

NAND



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR

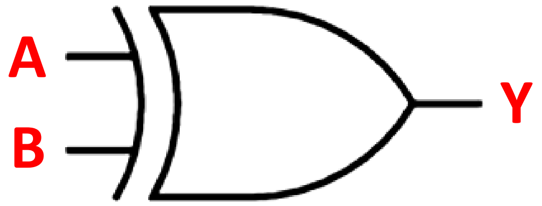


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

	INPUT	OUTPUT

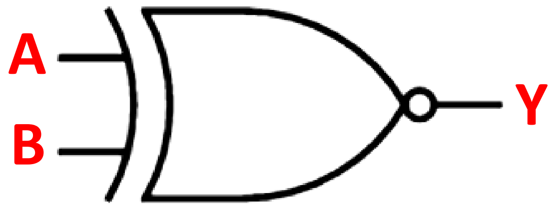
TRUTH TABLE

XOR
(exclusive OR)



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XNOR



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Boolean Algebra

Logic operations can be represented with formulas, using a special formalism called Boolean Algebra. The following table shows the Boolean notation.

OPERATOR	BOOLEAN ALGEBRA
NOT	$Y = \overline{A}$
AND	$Y = A\ B$
OR	$Y = A + B$
NAND	$Y = \overline{A\ B}$
NOR	$Y = \overline{A + B}$
XOR	$Y = A \oplus B$
XNOR	$Y = \overline{A \oplus B}$

NOTE: Some authors use $A.B$ for $A\ B$ and A' for $\overline{A}$

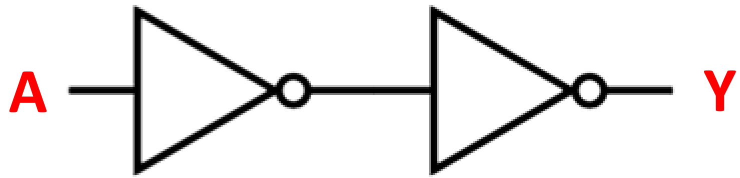
Boolean Algebra Simplifications Table

When a logic circuit is designed to obtain the desired behavior, it can be simplified by using the following laws to minimize the number of gates.

LAWS	AND	OR
Identity	$1\,A = A$	$0 + A = A$
Null	$0\,A = 0$	$1 + A = 1$
Idempotent	$A\,A = A$	$A + A = A$
Inverse	$A\,\overline{A} = 0$	$A + \overline{A} = 1$
Commutative	$A\,B = B\,A$	$A + B = B + A$
Associative	$(AB)C = A(BC)$	$(A + B) + C = A + (B + C)$
Distributive	$A + BC = (A + B)(A + C)$	$A(B + C) = AB + AC$
Absorption	$A(A + B) = A$	$A + AB = A$ $A + \overline{A}B = A + B$

Involution Law

$$\overline{\overline{A}} = A$$



AND VERY IMPORTANT:

De Morgan Theorem

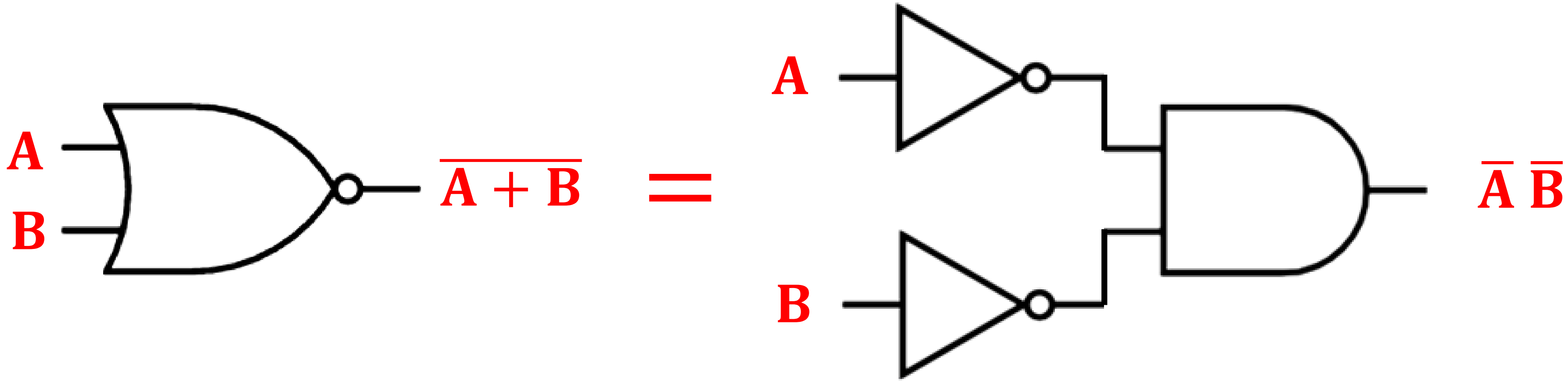
1) $$\overline{A + B} = \overline{A}\,\overline{B}$$

2) $$\overline{A\,B} = \overline{A} + \overline{B}$$

Circuit implementation

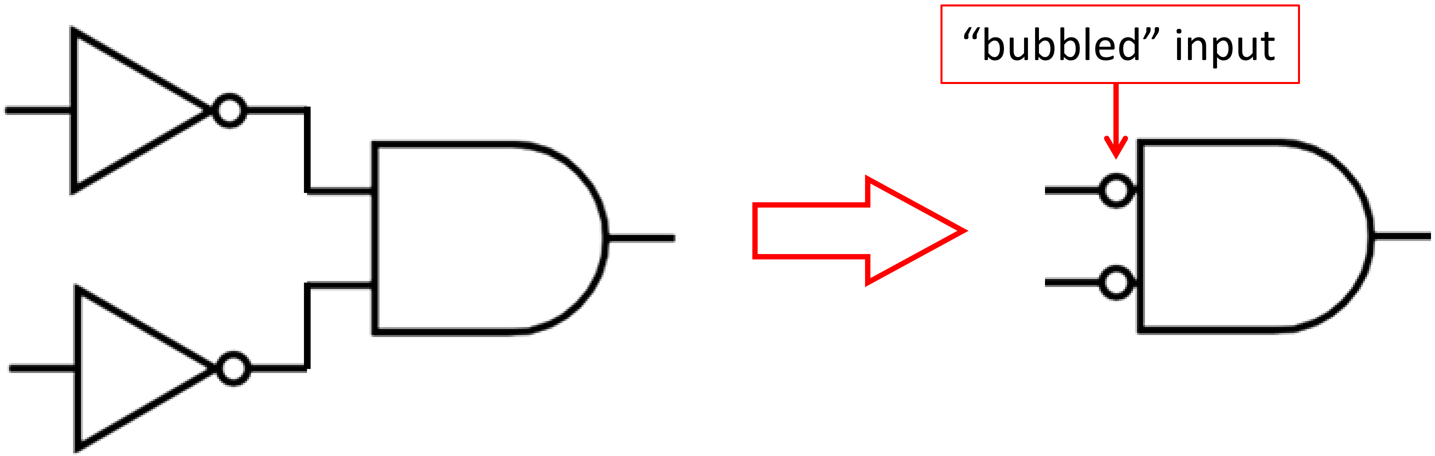
De Morgan Theorem

1) $$\overline{\mathbf{A}+\mathbf{B}} = \overline{\mathbf{A}}\,\overline{\mathbf{B}}$$

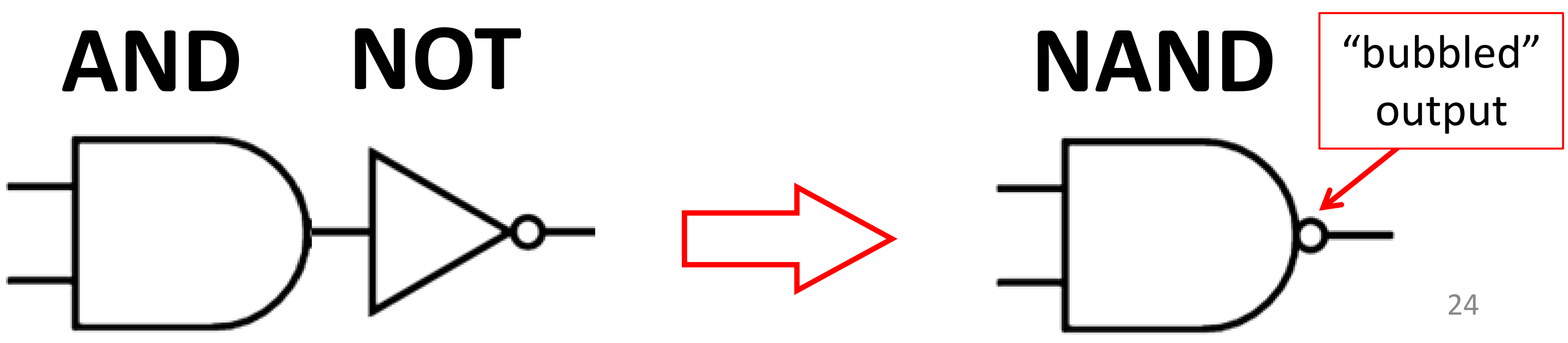


Note

In the practice it is not uncommon to simplify digital circuit layouts by expressing a NOT gate with a "bubble" in a connected element, for example :



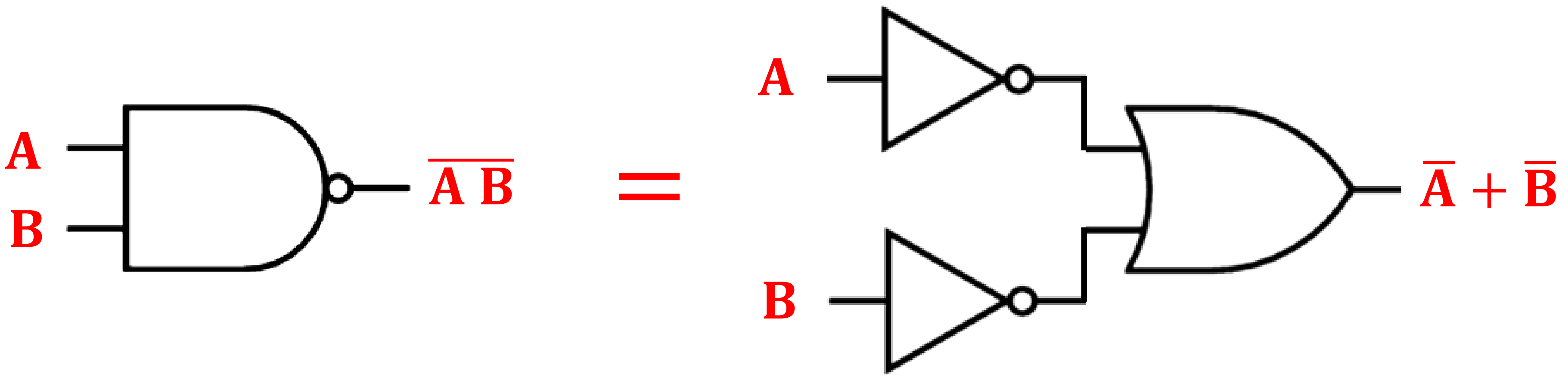
as done already in elementary gate definitions:



Circuit implementation

De Morgan Theorem

2) $\overline{\mathbf{A\,B}} = \overline{\mathbf{A}} + \overline{\mathbf{B}}$



AND Absorption Law (Proof)

$$\mathbf{A(A + B)}$$

Apply OR Distributive Law

$\mathbf{A(B + C) = AB + AC}$

$$\mathbf{AA + AB}$$

Apply Idempotent Law

$\mathbf{A\,A = A}$

$$\mathbf{A + AB}$$

Apply Identity Law

$\mathbf{1\,A = A}$

$$\mathbf{A1 + AB}$$

Apply OR Distributive Law

$\mathbf{A(B + C) = AB + AC}$

$$\mathbf{A(\underbrace{1 + B}_{= 1})}$$

Apply Null Law

$\mathbf{1 + A = 1}$

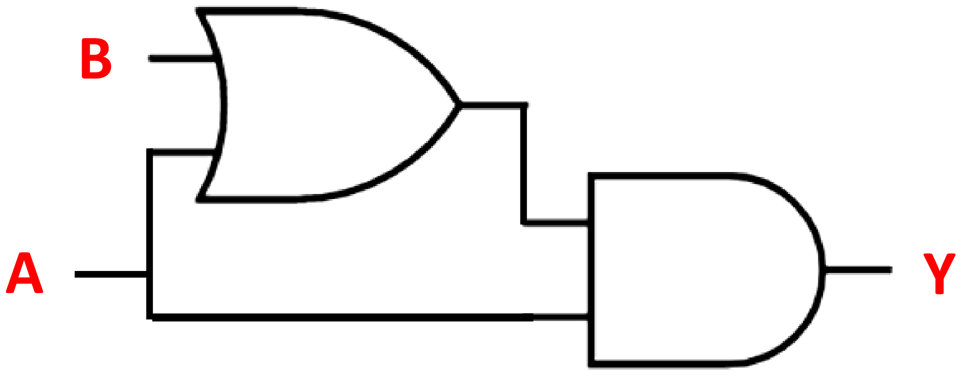
$$\mathbf{A(1)}$$

Apply Identity Law

$\mathbf{1\,A = A}$

$$\mathbf{A}$$

Logic Circuit Realization



$$\mathbf{A}(\mathbf{A} + \mathbf{B})$$

$$\mathbf{A}$$

AND Distributive Law (Proof)

$$(A + B)(A + C)$$

Apply OR Distributive Law twice

$A(B + C) = AB + AC$

$$AA + AC + BA + BC$$

Idempotent Law

$A\,A = A$

$$A + AC + BA + BC$$

Apply Commutative Law

Apply OR Absorption Law

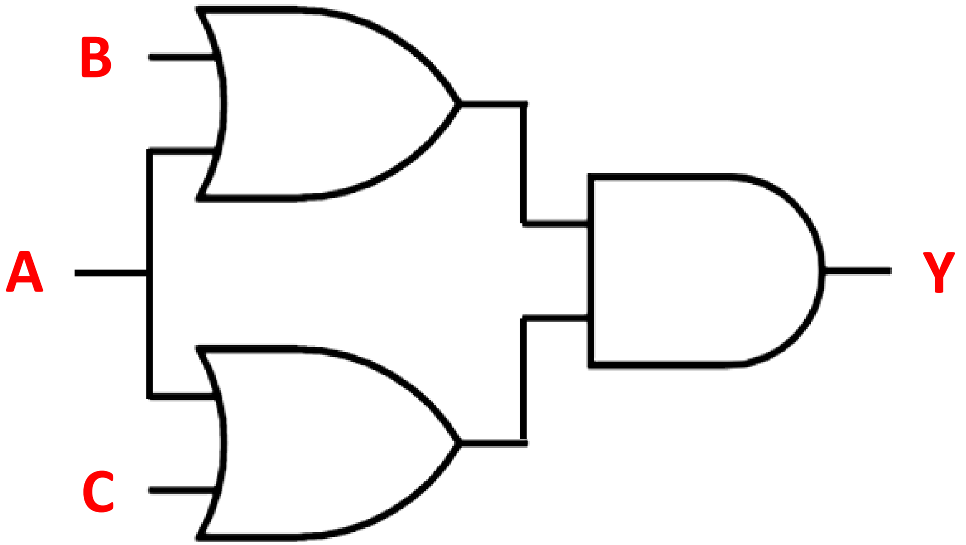
$A + AB = A$

$$A + AB + BC$$

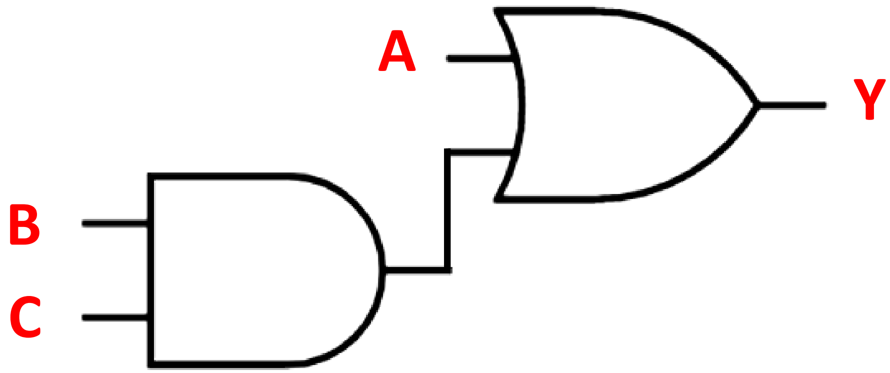
Apply OR Absorption Law

$$A + BC$$

Logic Circuit Realization



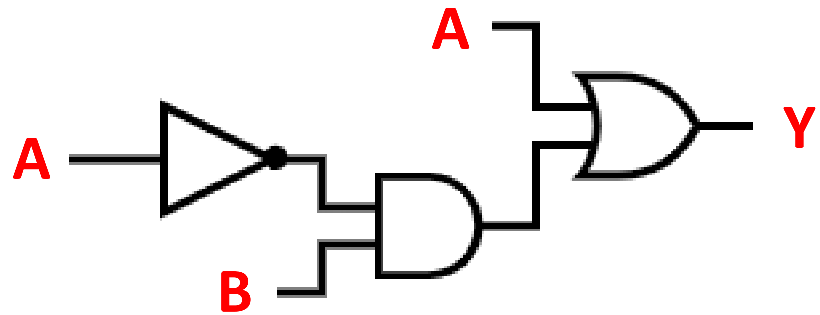
$$(\mathbf{A} + \mathbf{B})(\mathbf{A} + \mathbf{C})$$



$$\mathbf{A} + \mathbf{BC}$$

OR Absorption Law (Proof)

$$\mathbf{A} + \overline{\mathbf{A}}\,\mathbf{B}$$



Apply OR Distributive Law

$\mathbf{A} + \mathbf{BC} = (\mathbf{A} + \mathbf{B})(\mathbf{A} + \mathbf{C})$

$$(\mathbf{A} + \overline{\mathbf{A}})(\mathbf{A} + \mathbf{B})$$

Apply Null Law

$$\mathbf{1}(\mathbf{A} + \mathbf{B})$$

Apply Identity Law

$$\mathbf{A} + \mathbf{B}$$

Example 1

$$AB(\overline{B}C + AC)$$

Apply Distributive Law

$$AB\overline{B}C + ABAC$$

Apply Commutative Law

$$AB\overline{B}C + AABC$$

Apply Idempotent Law

$$AB\overline{B}C + ABC$$

Apply Inverse Law
(a.k.a. Complement Law)

$$A0C + ABC$$

Apply Null Law

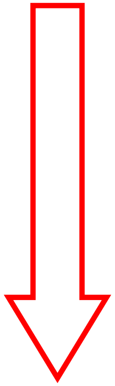
$$0 + ABC$$

Apply Identity Law

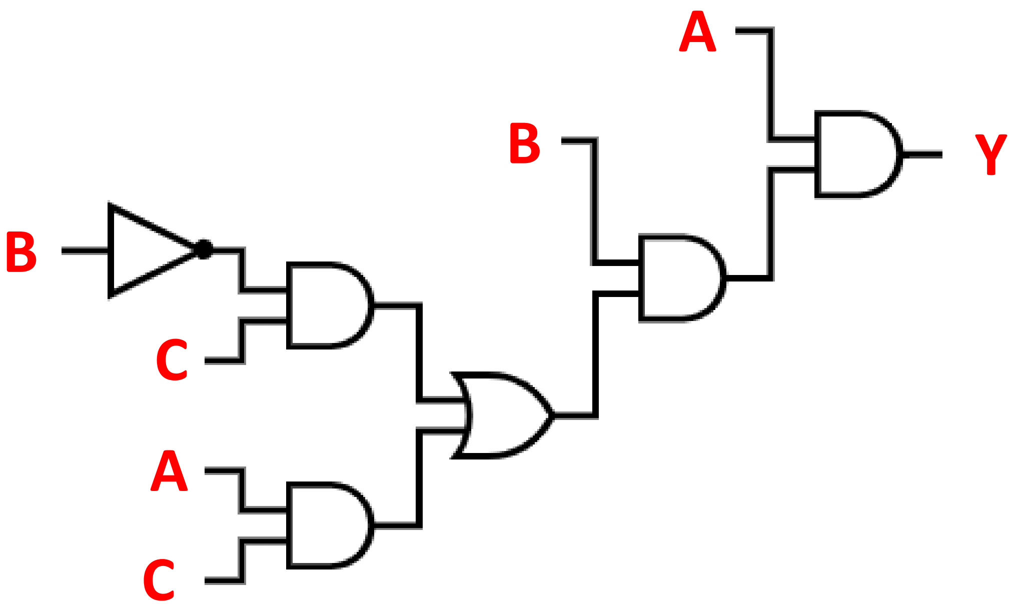
$$ABC$$

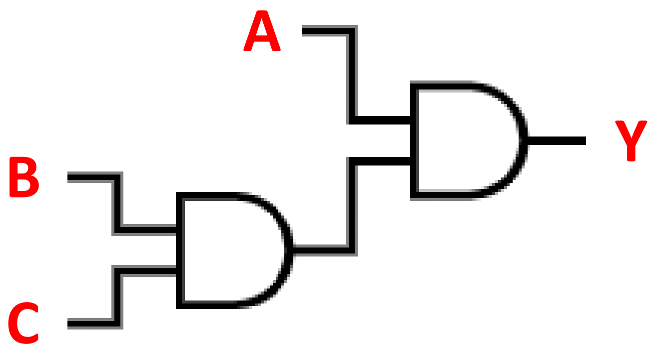
Example 1

$$AB(\bar{B}C + AC)$$



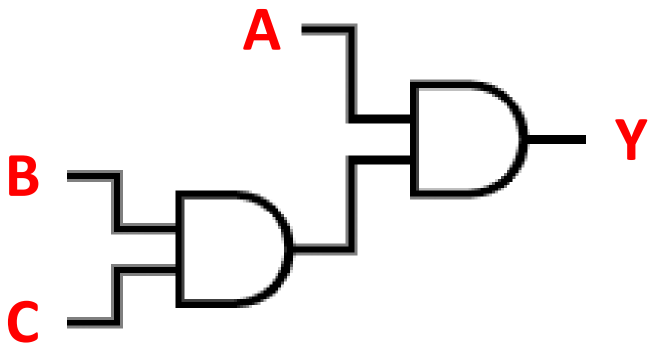
$$ABC$$





Example 1

ABC

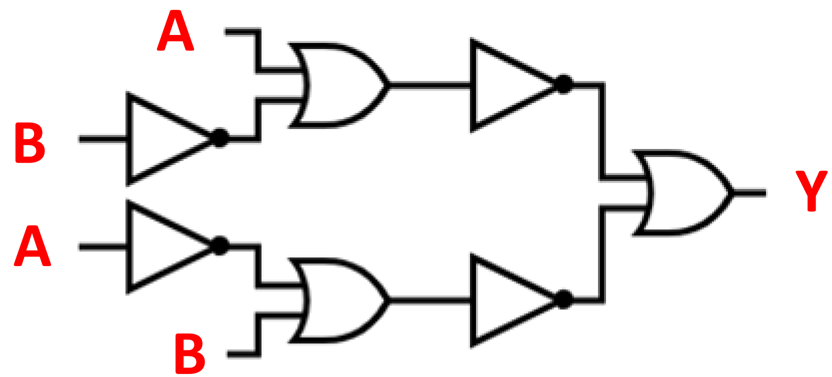


TRUTH TABLE

A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

Example 2

$$\overline{A + \overline{B}} + \overline{\overline{A} + B}$$



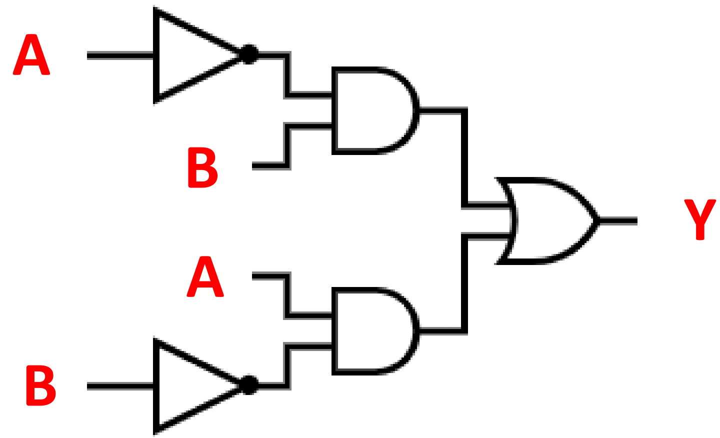
Apply De Morgan Theorem on both terms

$$\overline{A + B} = \overline{A}\,\overline{B}$$

$$\overline{A}\,\overline{\overline{B}} + \overline{\overline{A}}\,\overline{B}$$

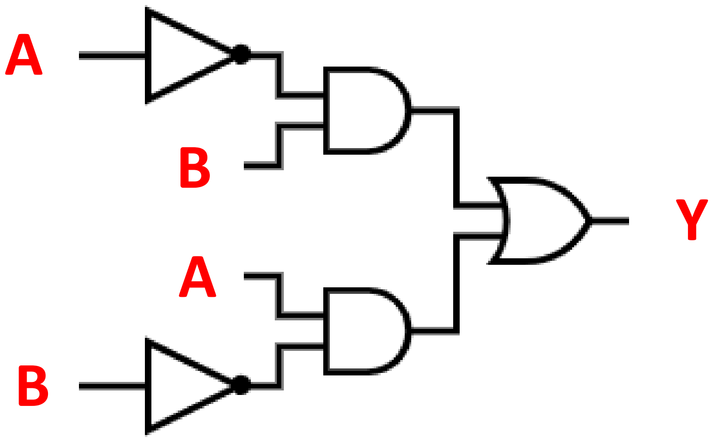
Apply Involution Law

$$\overline{A}\,B + A\,\overline{B}$$



Example 2

$$\bar{A}\,B + A\,\bar{B}$$



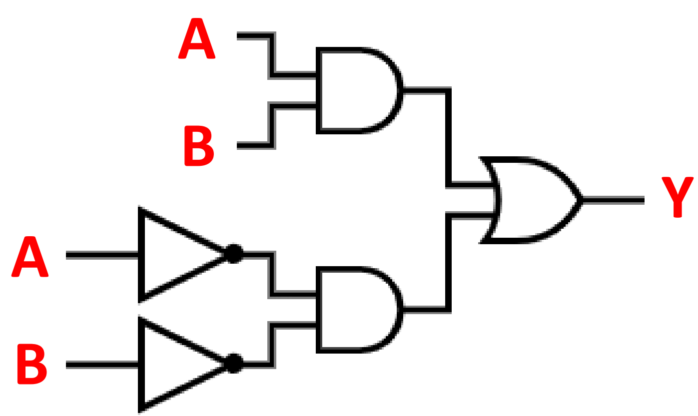
TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

This is the Truth Table of the XOR

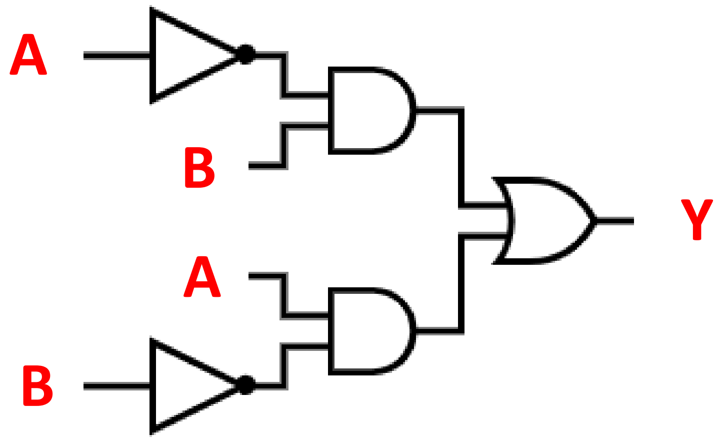
$$\overline{AB} + A\,B$$

An equivalent realization giving the same truth table



Example 2 Other equivalent circuits

$$\bar{A}\,B + A\,\bar{B}$$

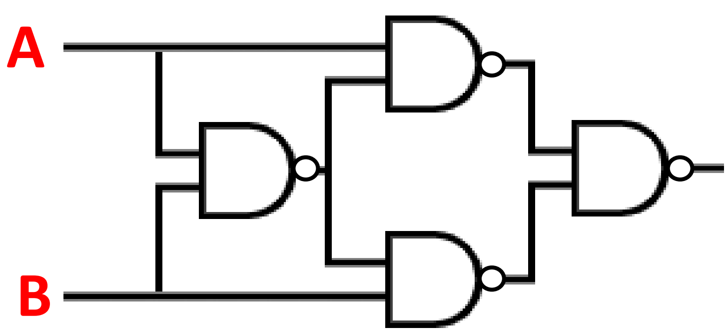


TRUTH TABLE

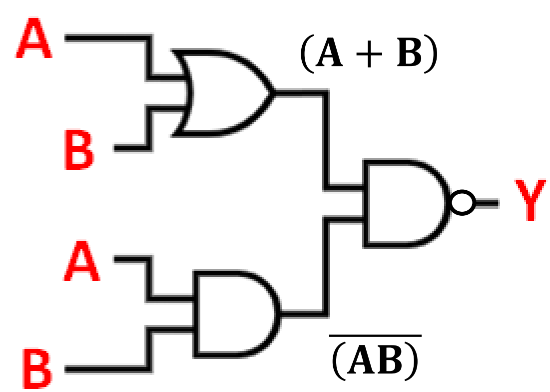
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

This is the Truth Table of the XOR

Realization only with NAND Gates



$$(A + B)\overline{(AB)}$$



Example 2

Prove

$$(A + B)\overline{(AB)} \Rightarrow \bar{A}\,B + A\,\bar{B}$$

Apply De Morgan Theorem

$$\overline{A\,B} = \bar{A} + \bar{B}$$

$$(A + B)(\bar{A} + \bar{B})$$

Apply Distribution Law

$$(\bar{A} + \bar{B})A + (\bar{A} + \bar{B})B$$

Apply Distribution Law

$$A\bar{A} + A\bar{B} + \bar{A}B + B\bar{B}$$

Apply Inverse Law

$$A\,\bar{A} = 0$$

$$0 + A\bar{B} + \bar{A}B + 0$$

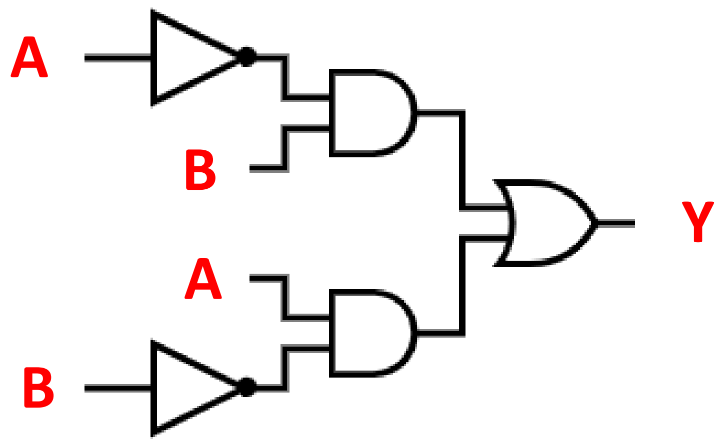
Apply Identity Law

$$0 + A = A$$

$$\bar{A}\,B + A\,\bar{B}$$

Example 2

$$\bar{A}\,B + A\,\bar{B}$$



TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

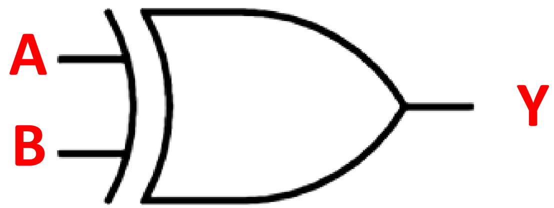
This is the Truth Table of the XOR

$$Y = A \oplus B$$

We have just designed one possible logic circuit to operate a light with two switches

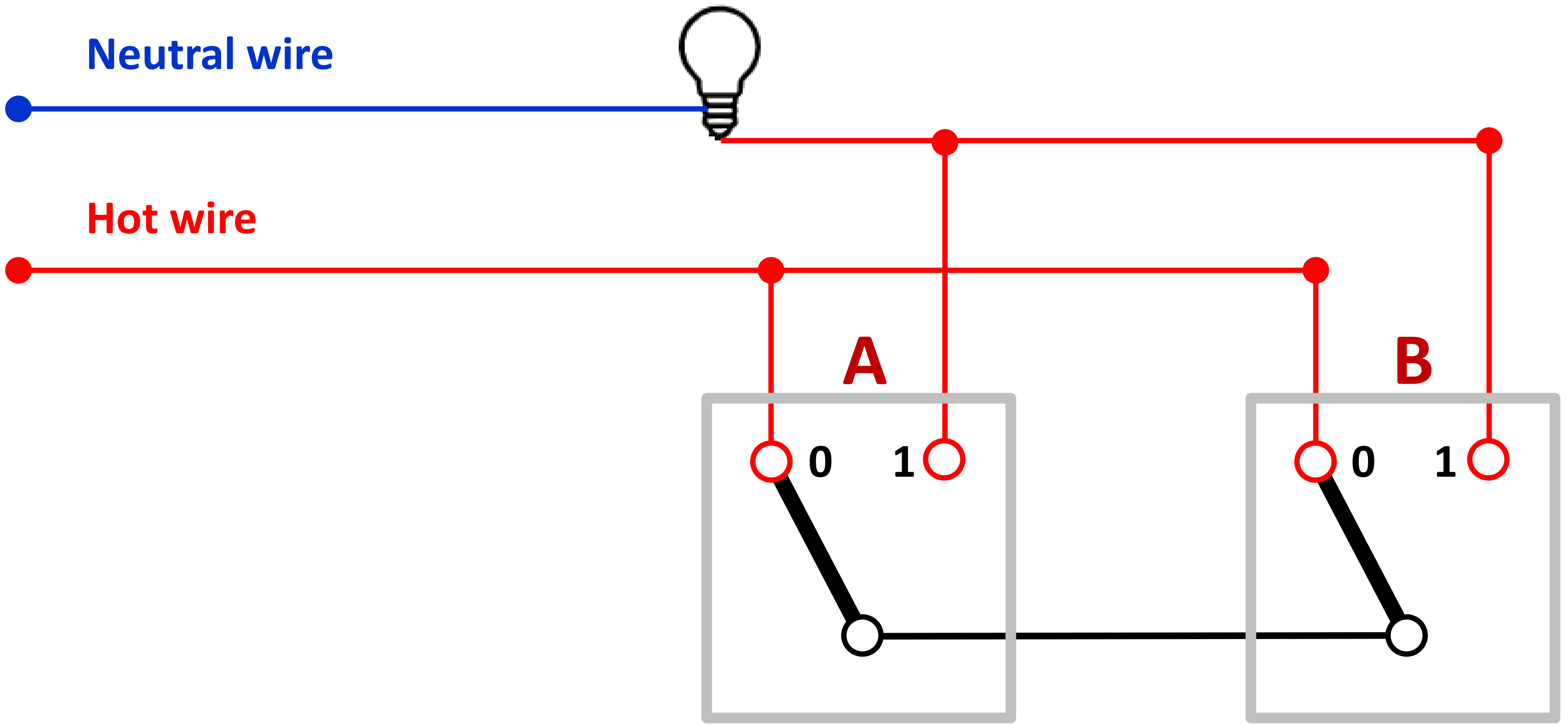
Example 2

Here is how an electrician implements the wiring of XOR with two-way switches



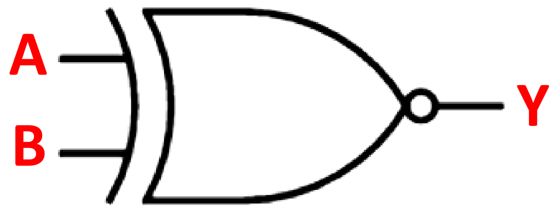
TRUTH TABLE

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



Example 2

Here is how an electrician implements the wiring of XNOR with two-way switches



TRUTH TABLE

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1