ECE 205 “Electrical and Electronics Circuits”

Spring 2024 – LECTURE 31

MWF – 12:00pm

Prof. Umberto Ravaioli

2062 ECE Building

Lecture 31 – Summary

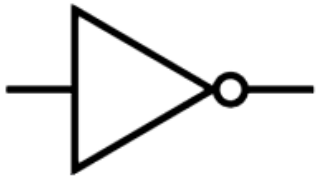
Learning Objectives

1. **Universal gates combine to realize any other logic function**
2. **Logic gates realized physically with BJT's**

Using standard gates to construct other logic functions

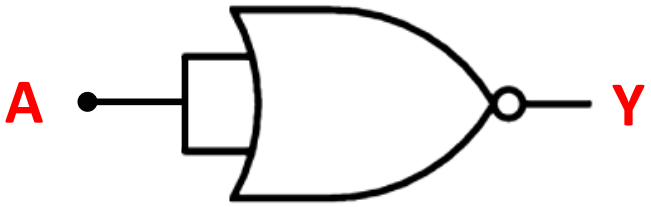
NOR and NAND are considered universal gates for the purpose of constructing other ones.

Construct the NOT gate

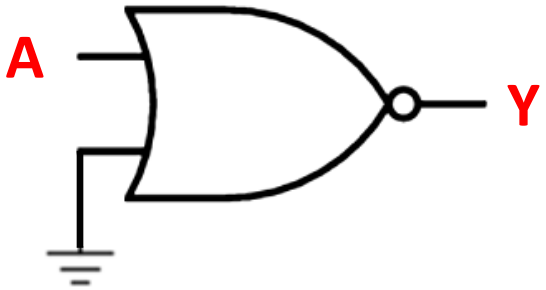


NOT

A	Y
0	1
1	0

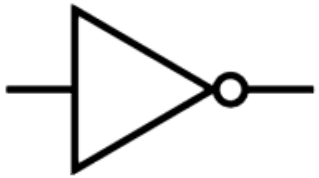


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



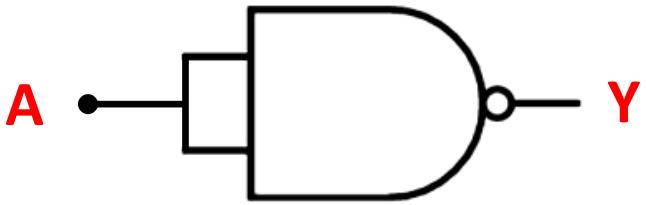
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Construct the NOT gate

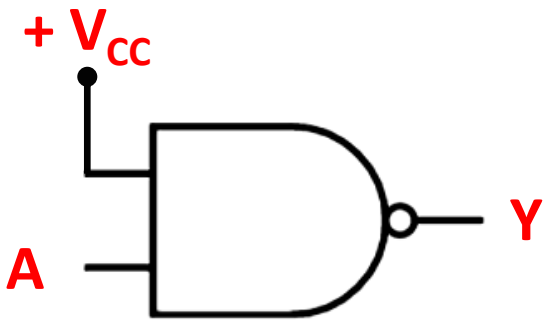


NOT

A	Y
0	1
1	0

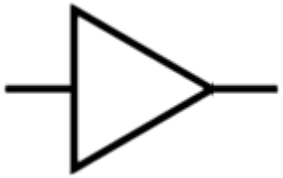


A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



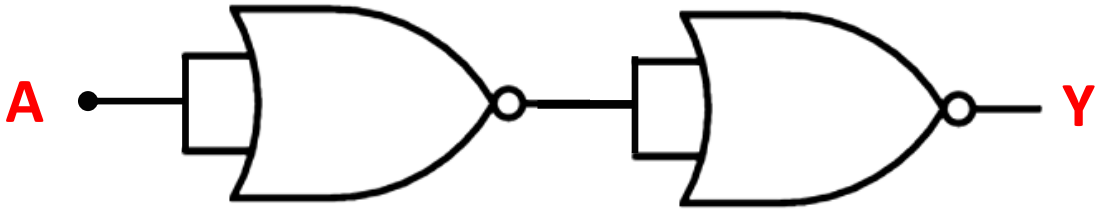
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

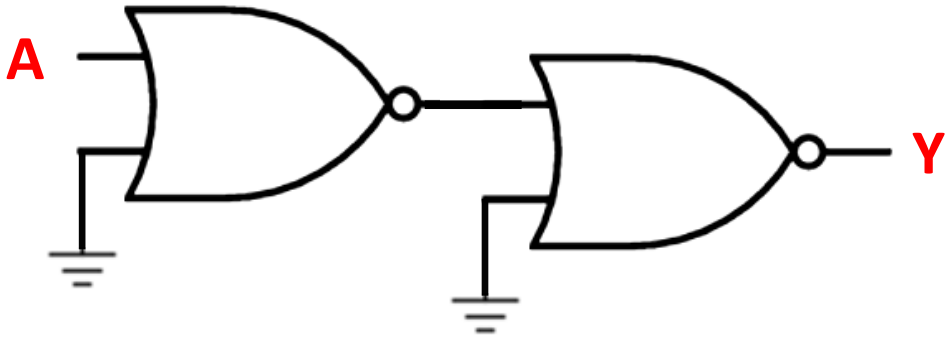
Construct the BUFFER gate



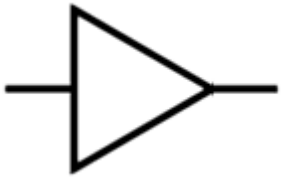
BUFFER

A	Y
0	0
1	1



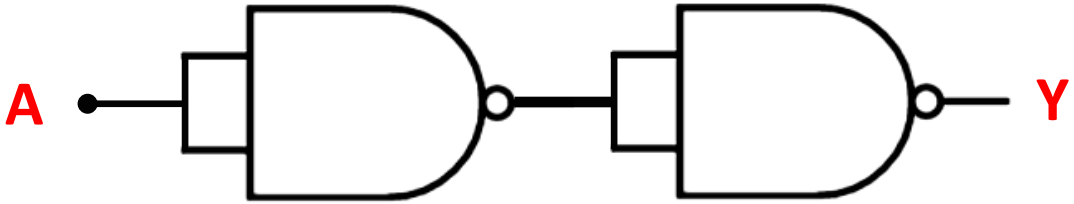


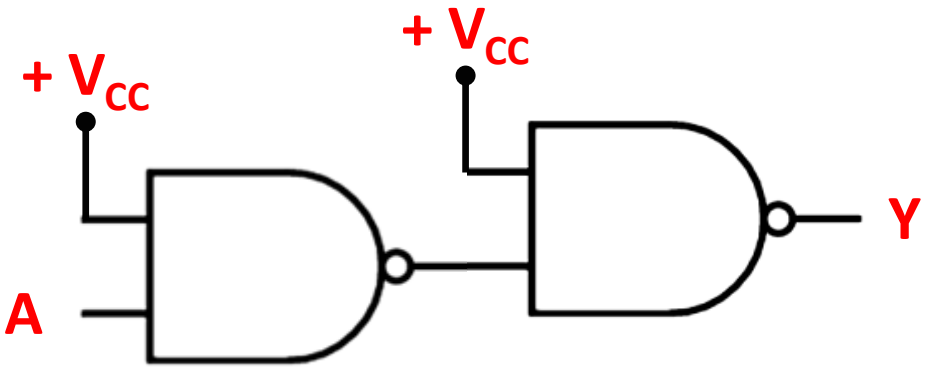
Construct the BUFFER gate



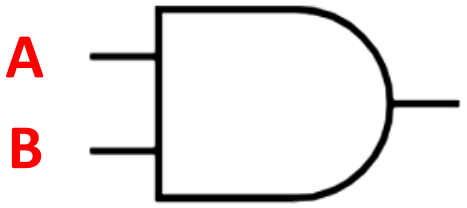
BUFFER

A	Y
0	0
1	1





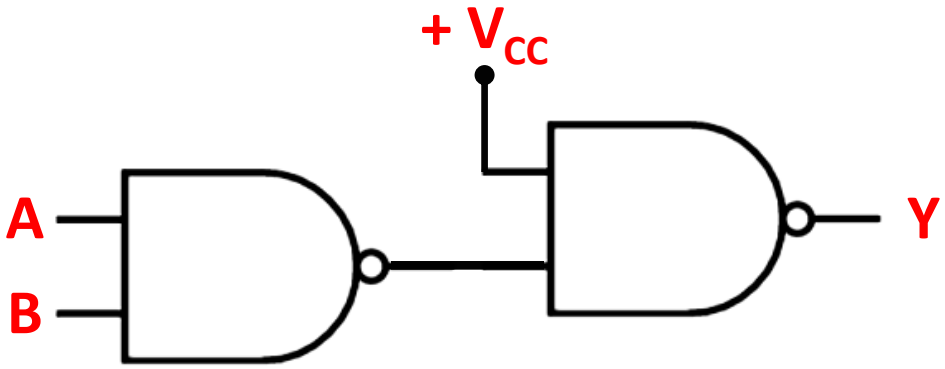
Construct the AND gate



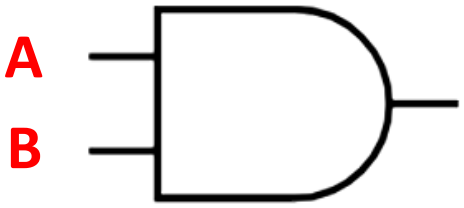
AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Use NAND gates



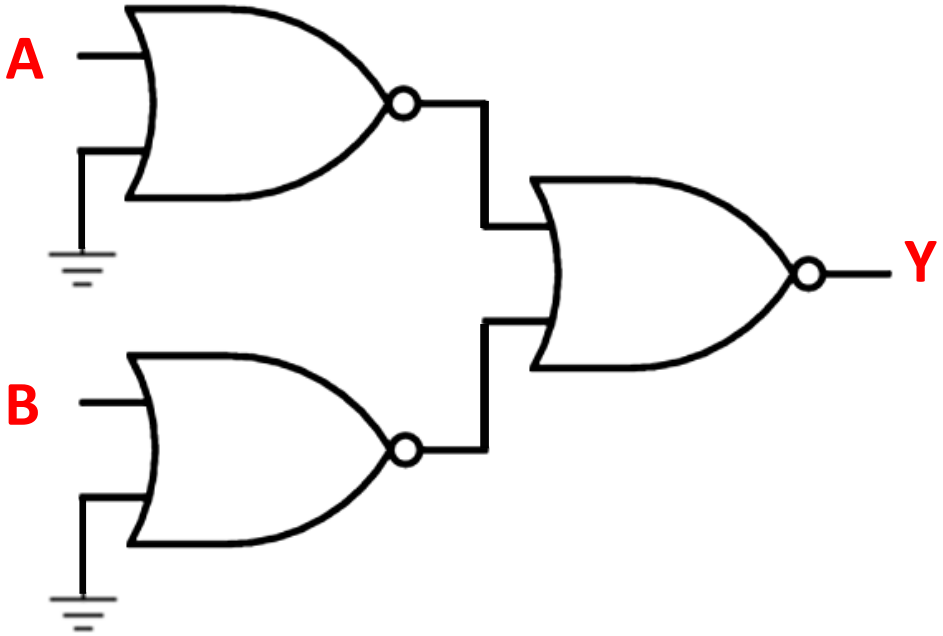
Construct the AND gate



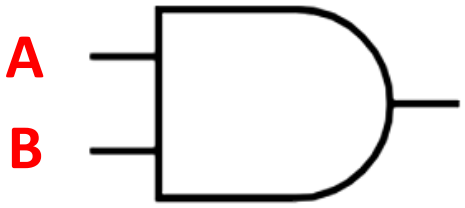
AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Use NOR gates

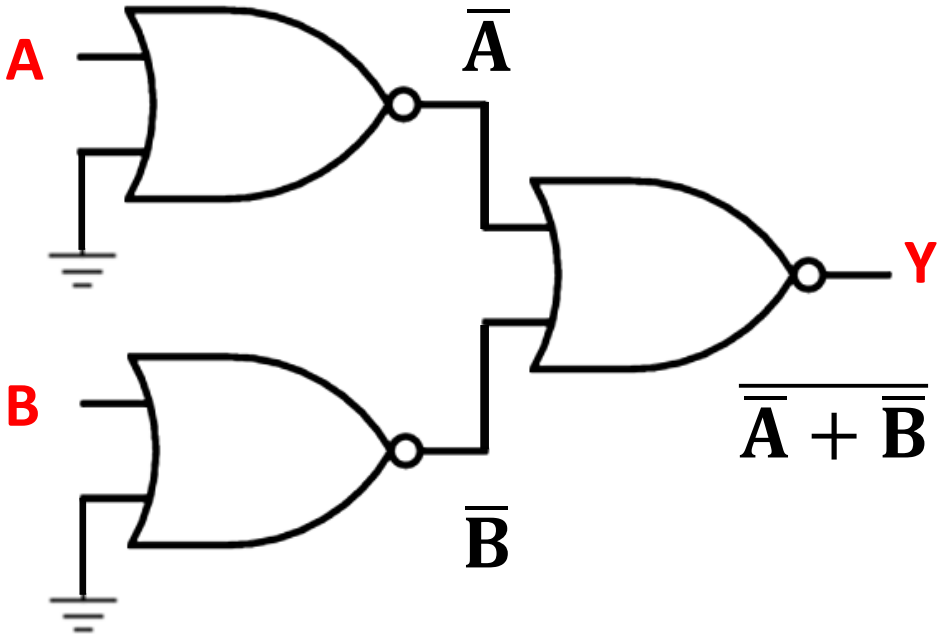


Construct the AND gate



AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



PROOF

$$Y = \overline{\overline{A} + \overline{B}}$$

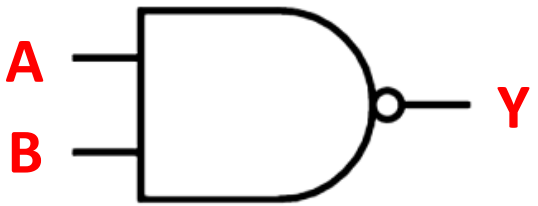
Apply De Morgan Theorem

$$\overline{A} + \overline{B} = \overline{A\,B}$$

$$Y = \overline{\overline{A\,B}} = A\,B$$

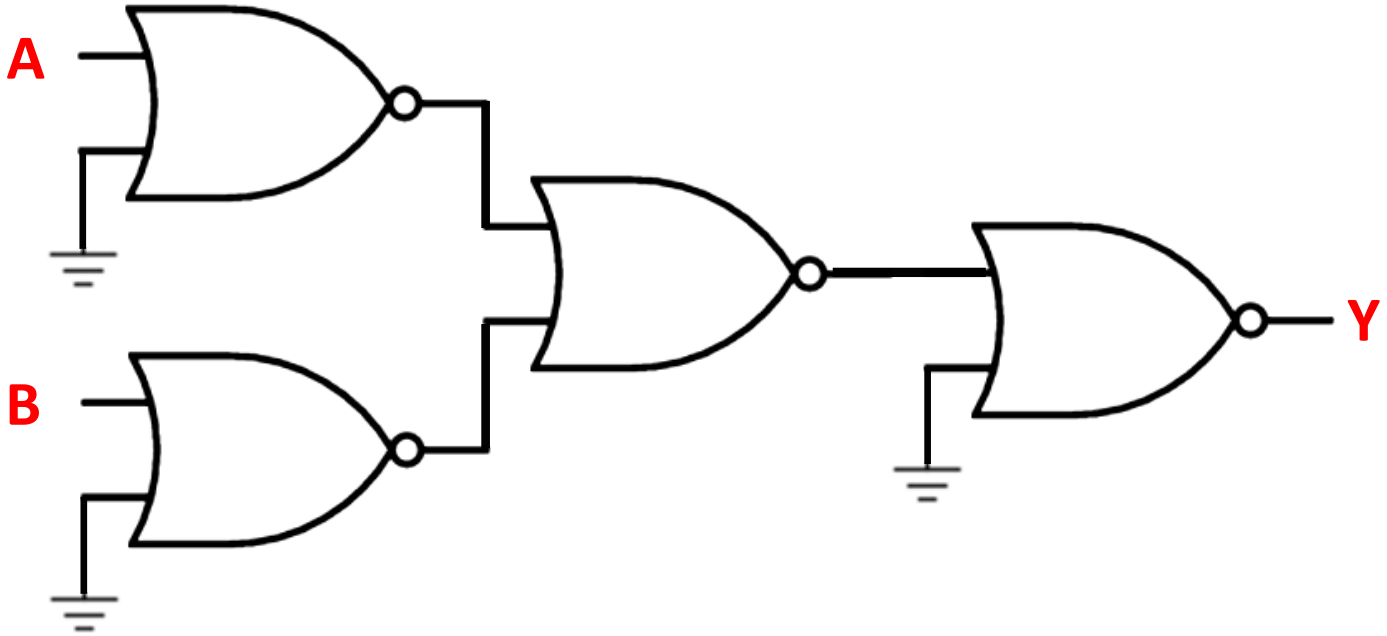
Apply Involution Law

Construct the NAND gate

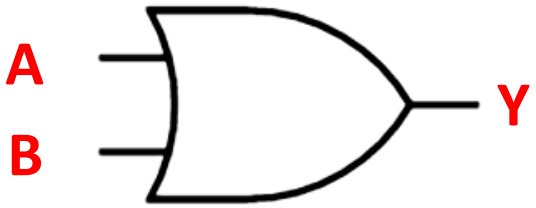


NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



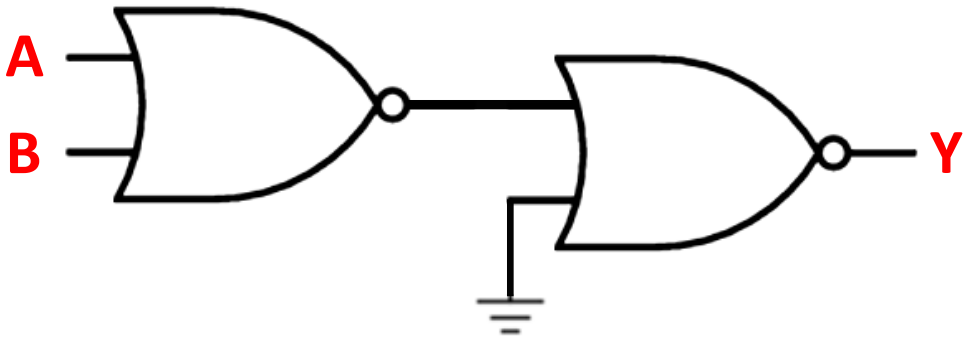
Construct the OR gate



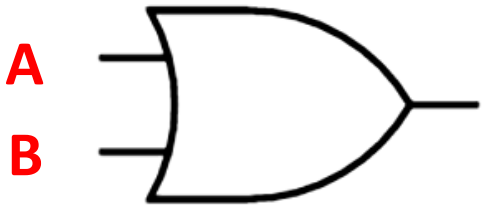
OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Use NOR gates



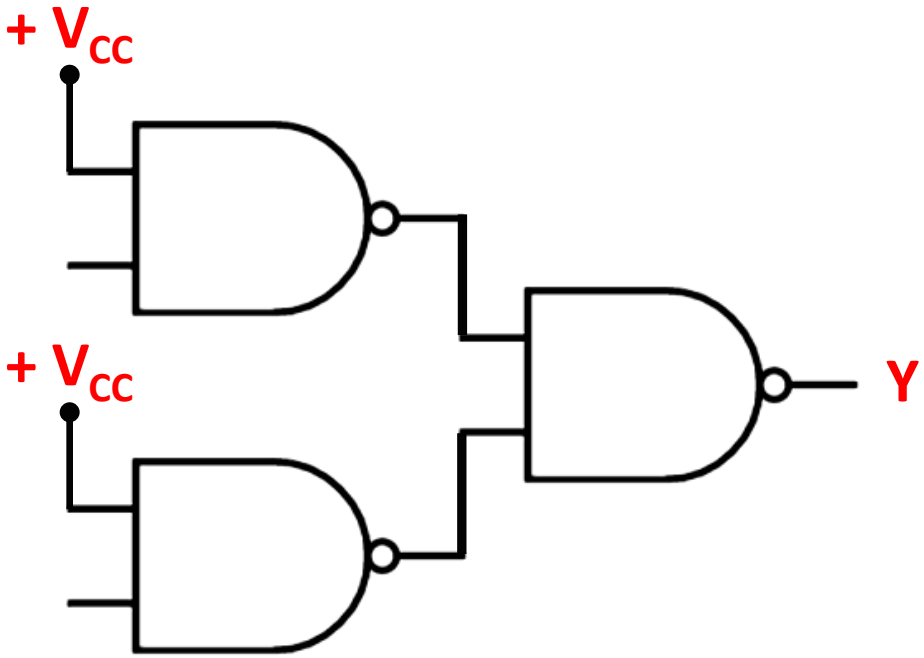
Construct the OR gate



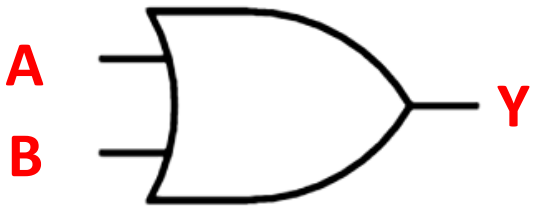
OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Use NAND gates

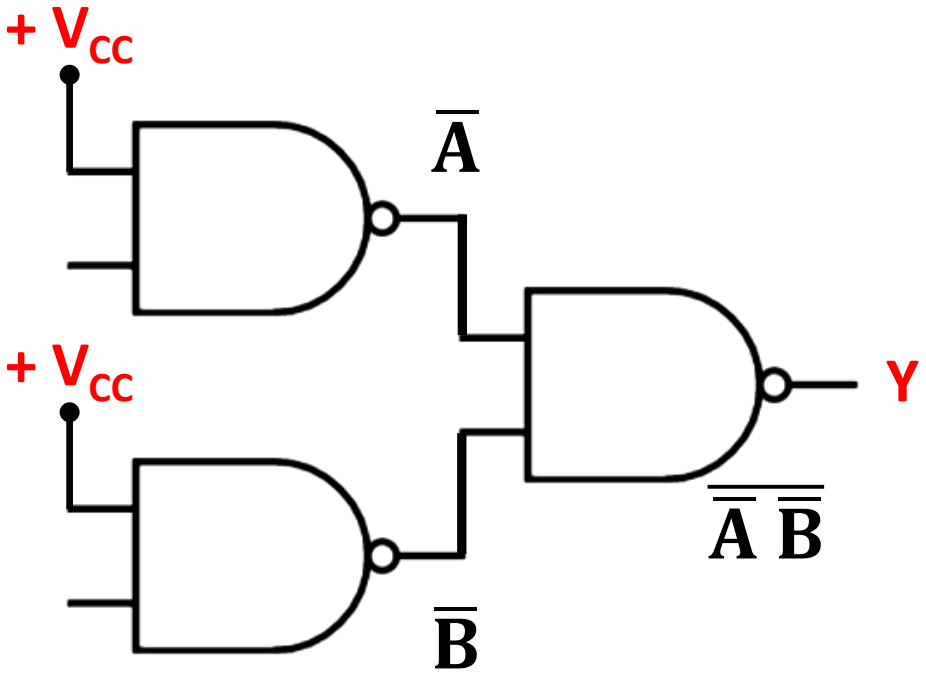


Construct the OR gate



OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



PROOF

$$Y = \overline{\overline{A}\,\overline{B}}$$

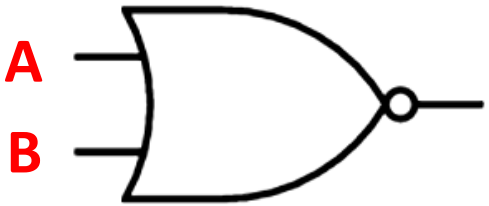
Apply De Morgan Theorem

$$\overline{A}\,\overline{B} = \overline{A + B}$$

$$Y = \overline{\overline{A + B}} = A + B$$

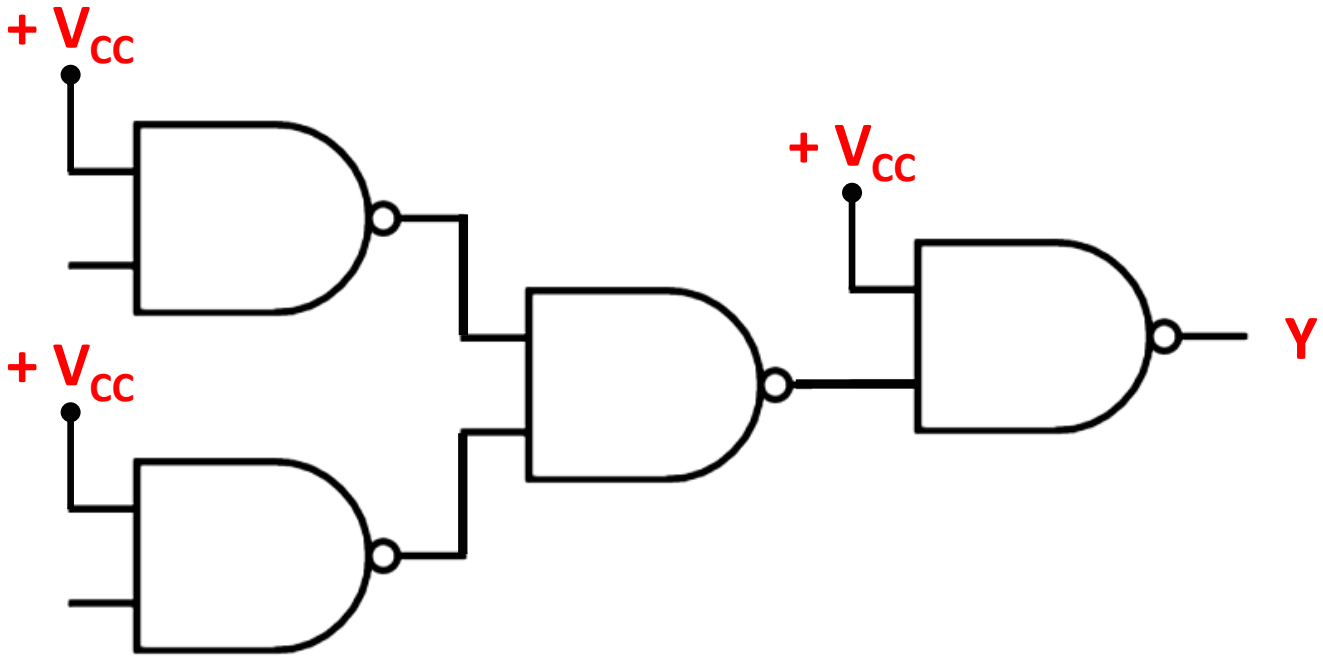
Apply Involution Law

Construct the NOR gate



NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

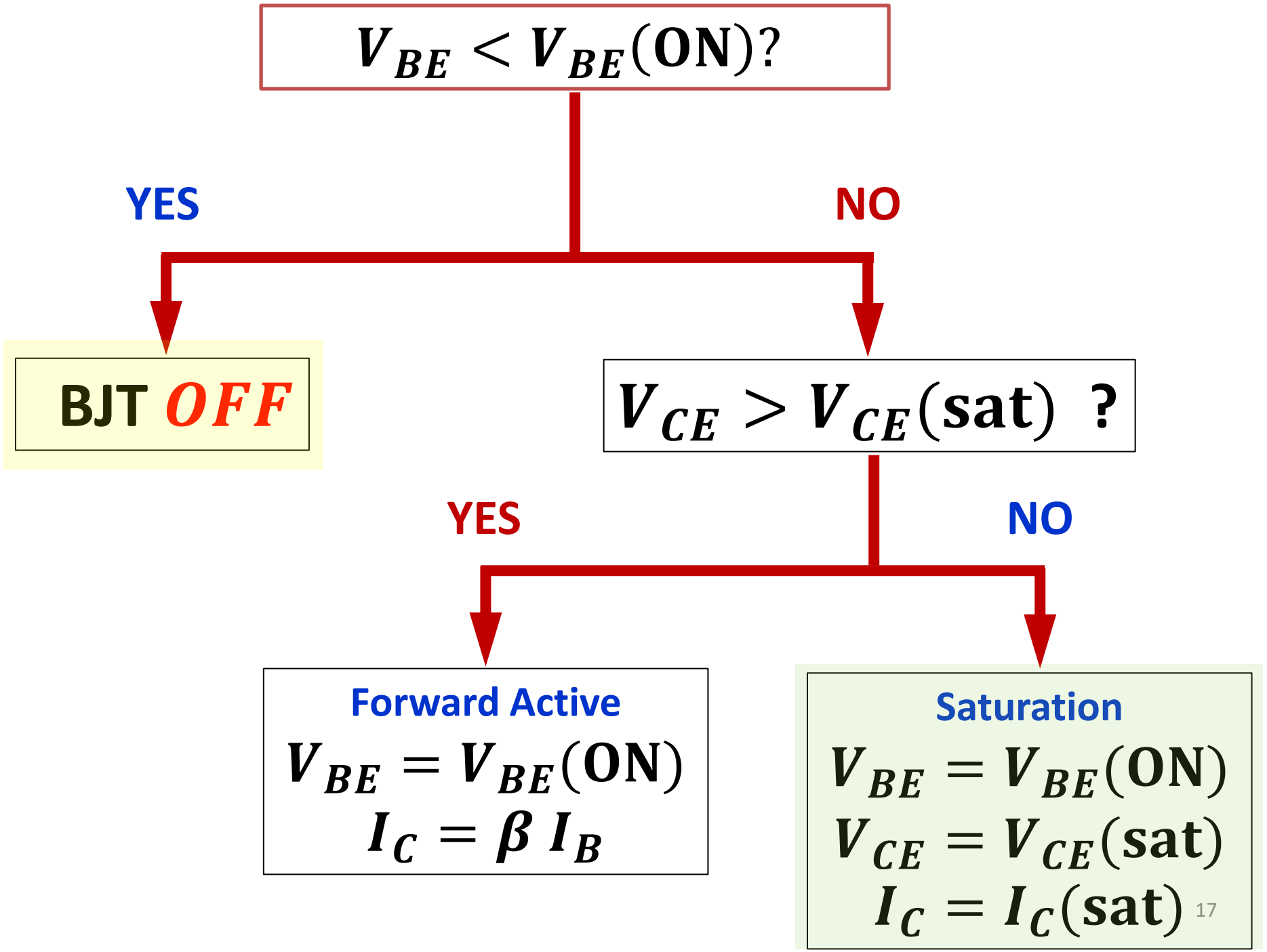


Logic Gates using BJT's

We consider logic gates made with BJTs connected by resistors (Resistor-Transistor-Logic or RTL). This was the earliest digital logic family for integrated circuits.

While there are much higher performance designs for BJT chips (e.g., Transistor-Transistor-Logic or TTL), RTL is still a good approach to prototype simple logic circuits with discrete components that can handle a fair amount of power in servo-mechanisms.

Intermediate between RTL and TTL, there was the Diode-Transistor-Logic (DTL) where inputs run through *p-n* junctions.

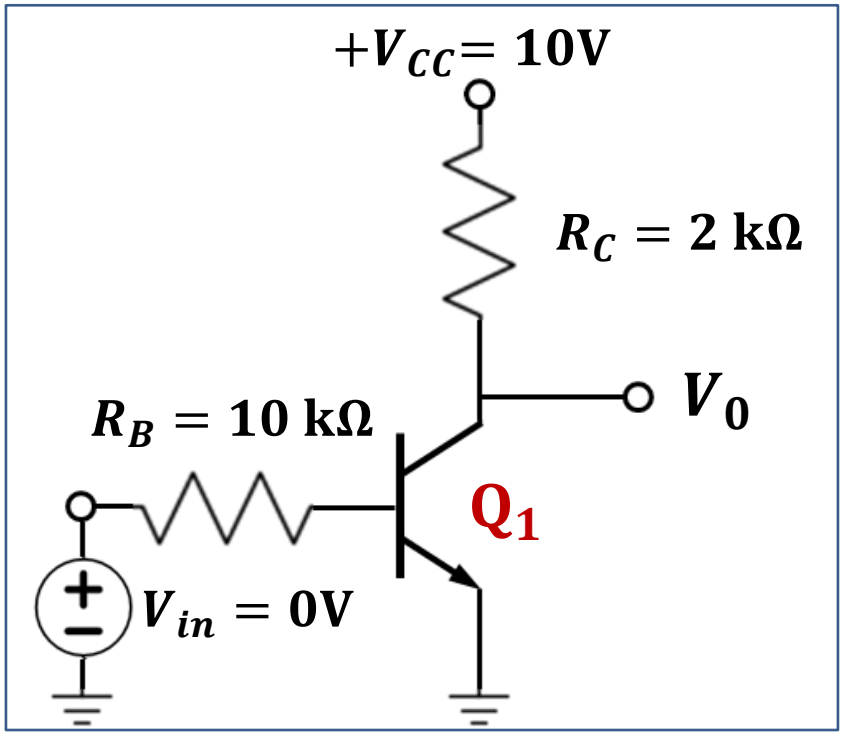

$V_{BE} < V_{BE}(\mathrm{ON})?$
YES
NO
BJT OFF
$V_{CE} > V_{CE}(\mathrm{sat})$?
YES
NO
Forward Active
$V_{BE} = V_{BE}(\mathrm{ON})$
$I_C = \beta I_B$
Saturation
$V_{BE} = V_{BE}(\mathrm{ON})$
$V_{CE} = V_{CE}(\mathrm{sat})$
$I_C = I_C(\mathrm{sat})$

Consider two cases

Assume $V_{BE}(\mathrm{ON}) = 0.7\ \mathrm{V}$

$V_{CE}(\mathrm{sat}) = 0.2\ \mathrm{V}$

$\beta = 10$



$V_{BE} < V_{BE}(\mathrm{ON})$

$V_0 = V_{CC} = 10\mathrm{V}$

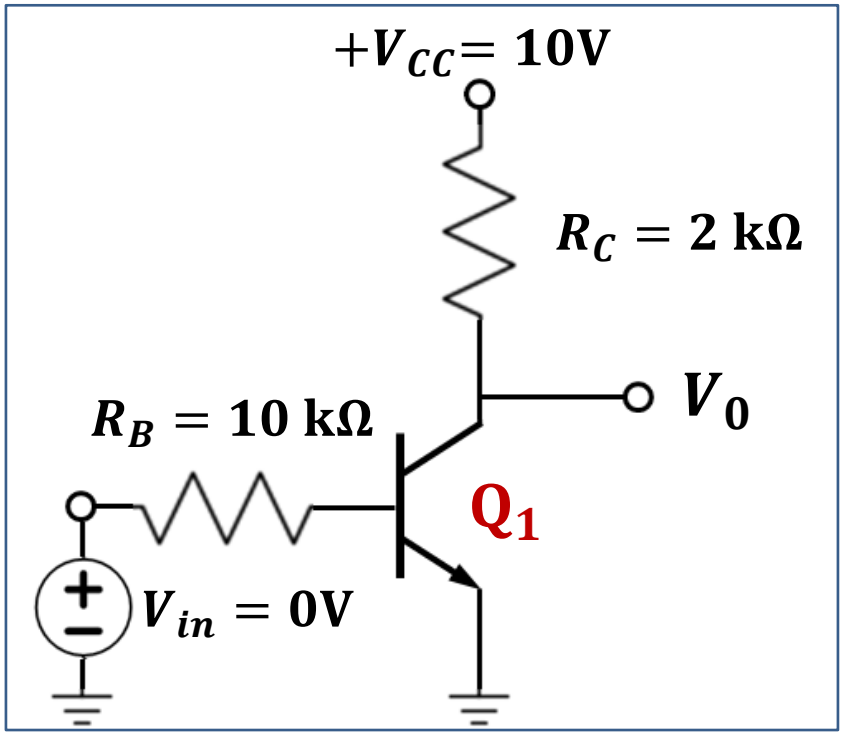
Q_1 OFF

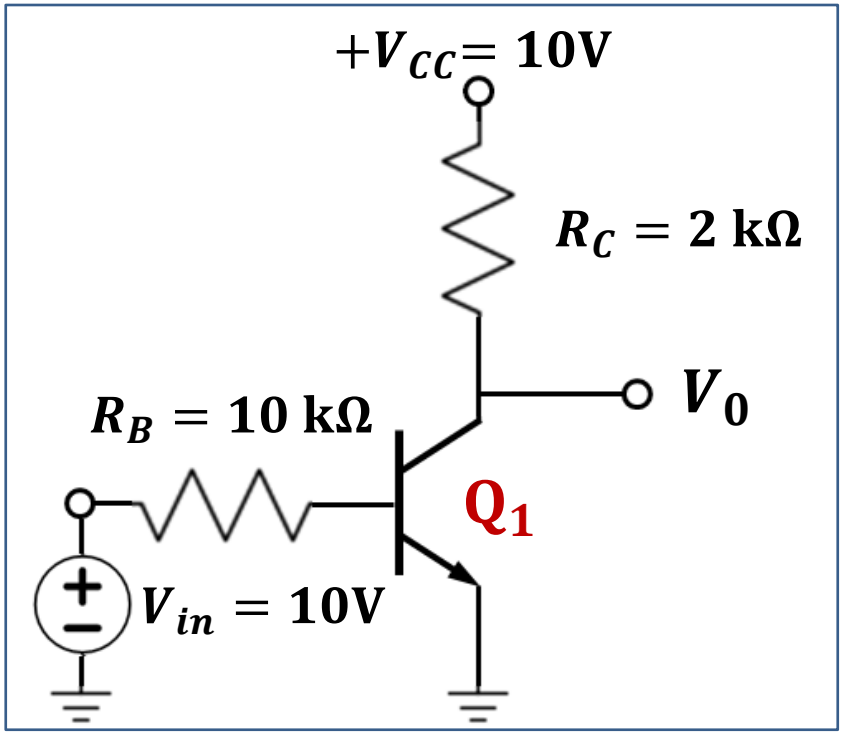
Consider two cases

Assume $V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$





$V_{BE} < V_{BE}(\text{ON})$

$V_0 = V_{CC} = 10\text{V}$

Q_1 OFF

$$I_B = \frac{10 - 0.7}{10\text{k}\Omega} = 0.93\text{mA}$$

$I_C = \beta I_B = 9.3\text{mA}$ Assuming FA mode

$$I_C(\text{sat}) = \frac{10 - 0.2}{2\text{k}\Omega} = 4.8\text{mA}$$

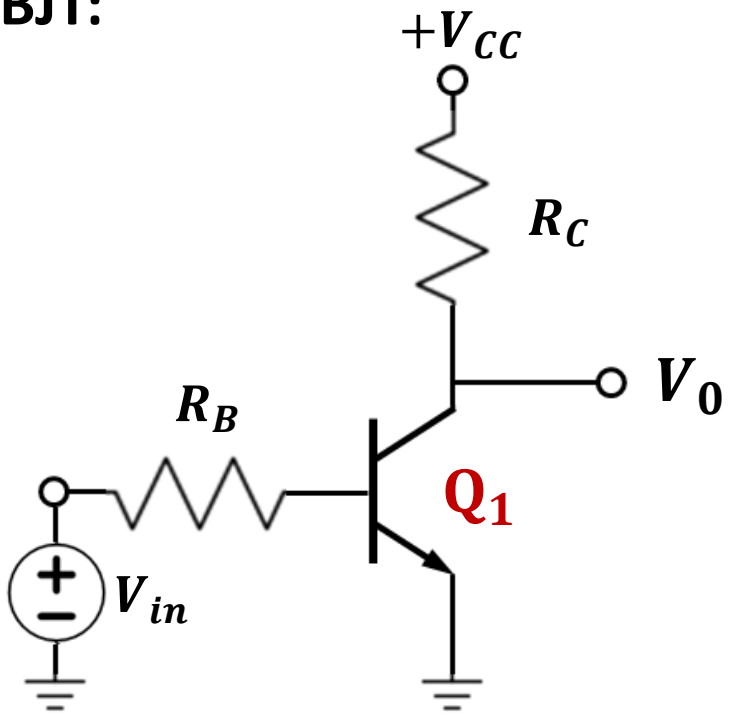
Q_1 SATURATION $V_0 = 0.2\ \text{V}$

Basic principle to design logic gates with BJT:

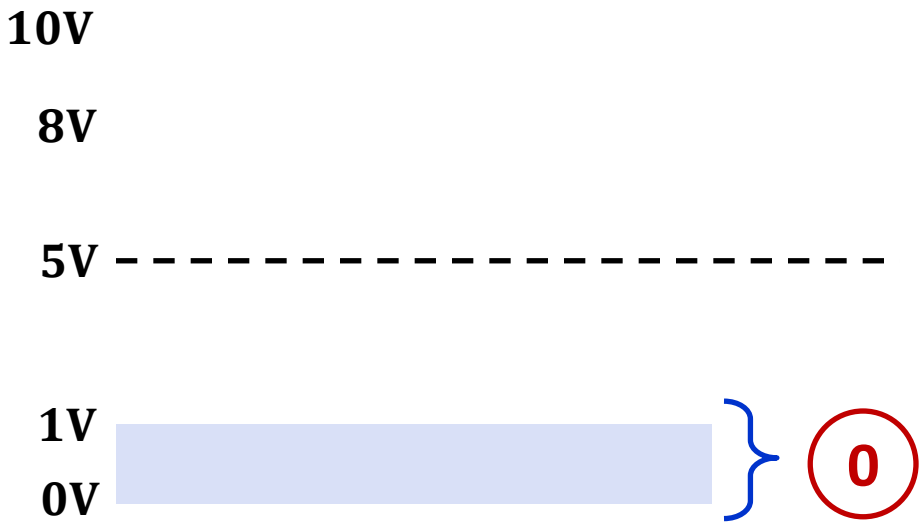
Two states of operation

(0) LOW $V_{in} \rightarrow$ HIGH V_0 (1)

Q_1 OFF



For a given technology one has to set reference voltage levels to accept logical states 0 and 1.



Basic principle to design logic gates with BJT:

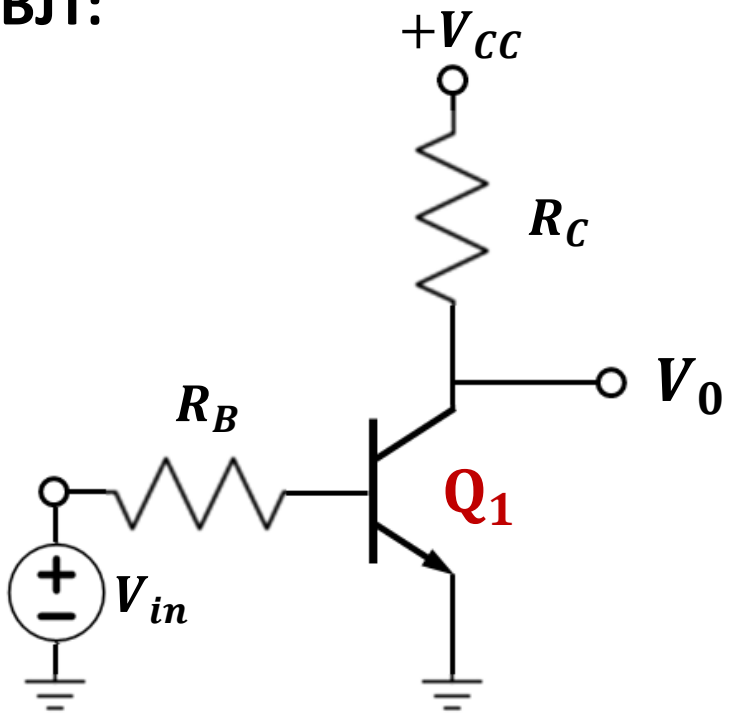
Two states of operation

(0) LOW $V_{in} \rightarrow$ HIGH V_0 (1)

Q_1 OFF

(1) HIGH $V_{in} \rightarrow$ LOW V_0 (0)

Q_1 SATURATION



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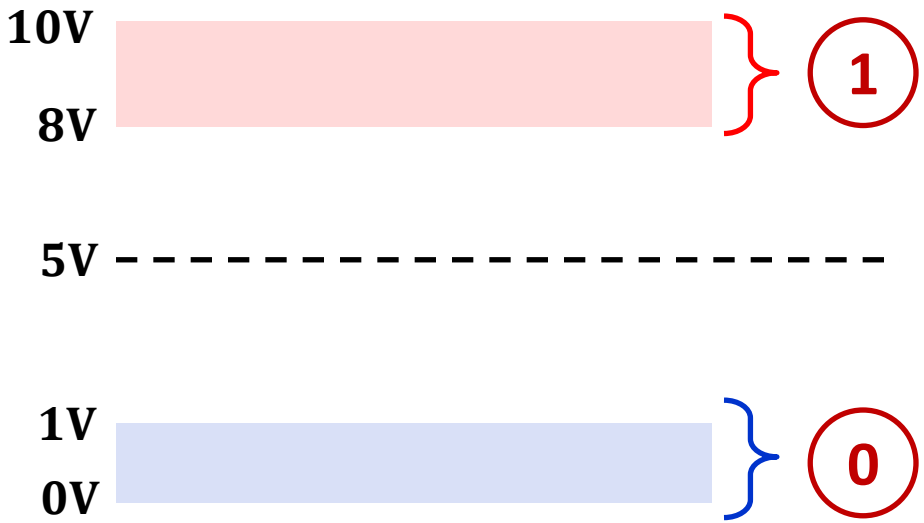
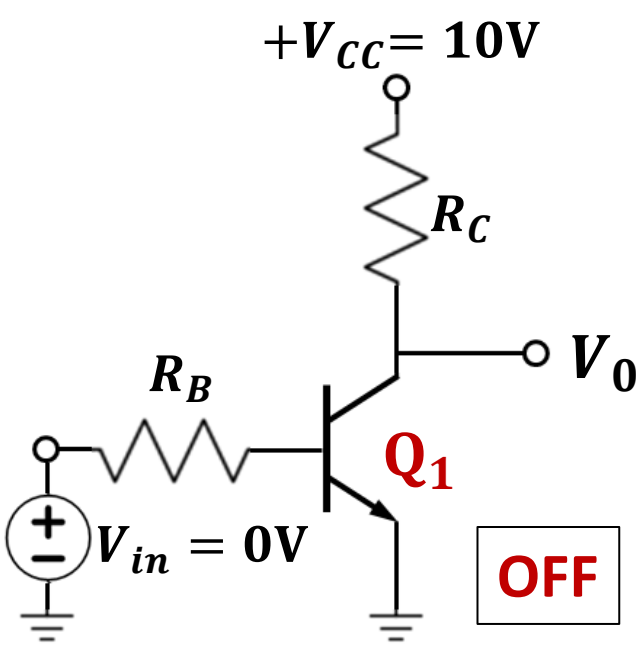
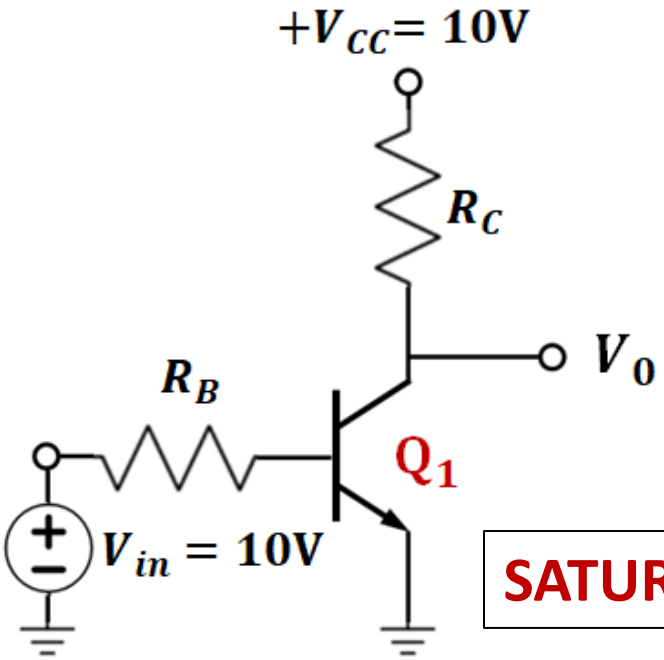


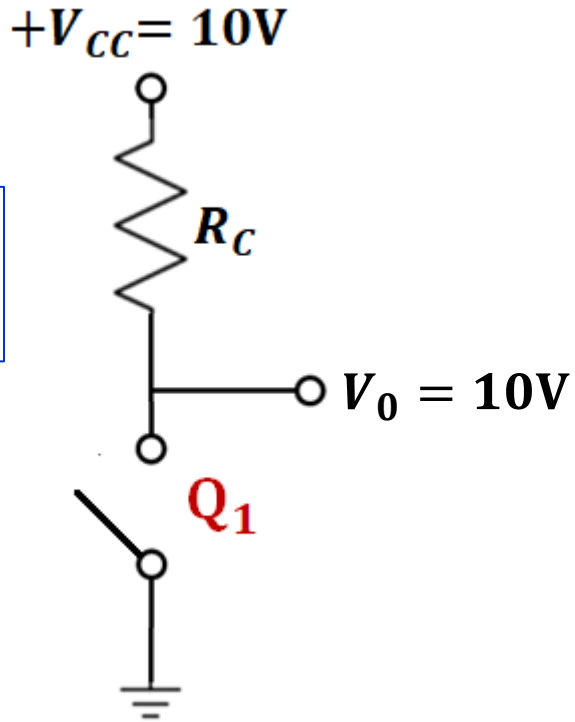


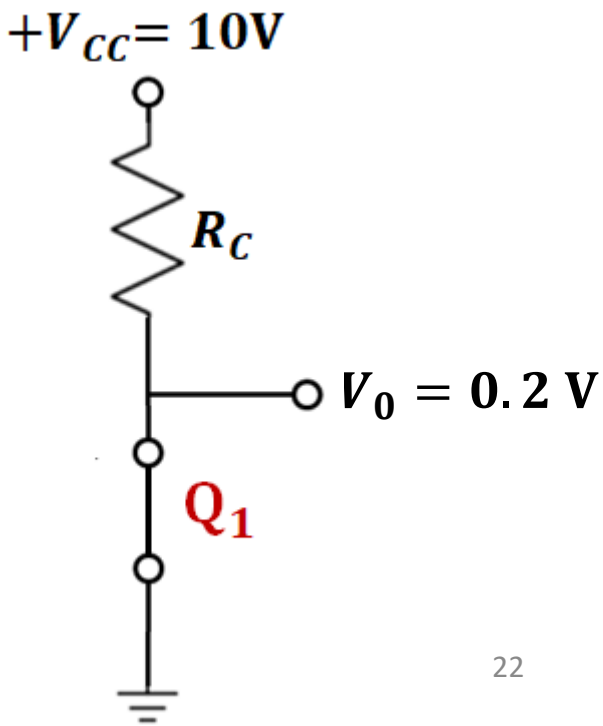
OFF



SATURATION

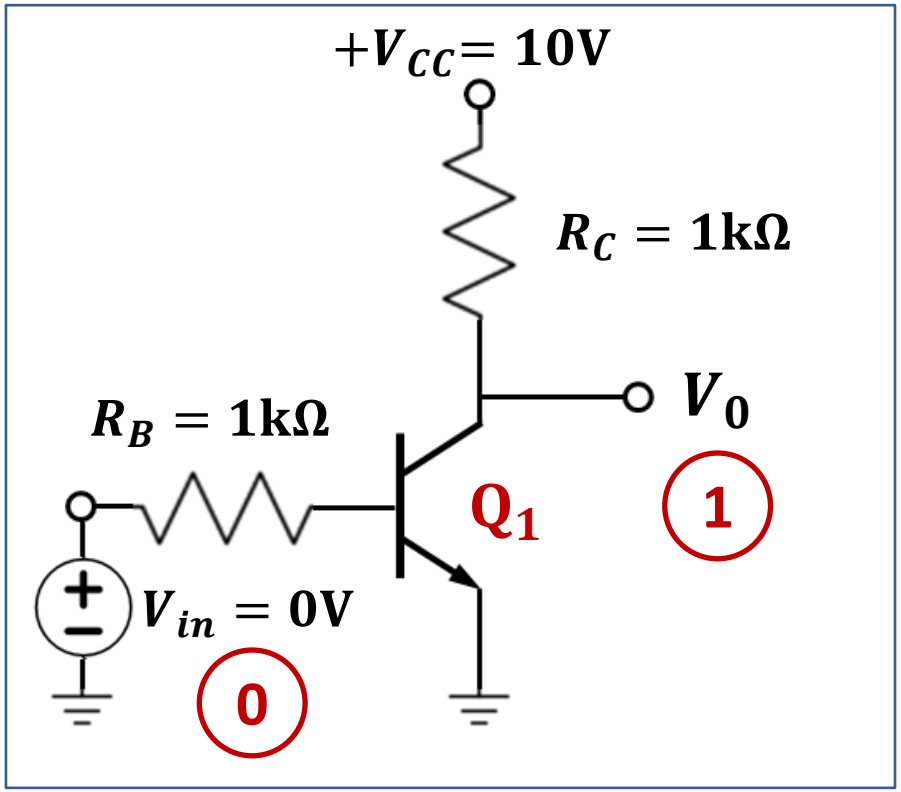
Transistors are like switches





Basic Inverter (NOT) implementation

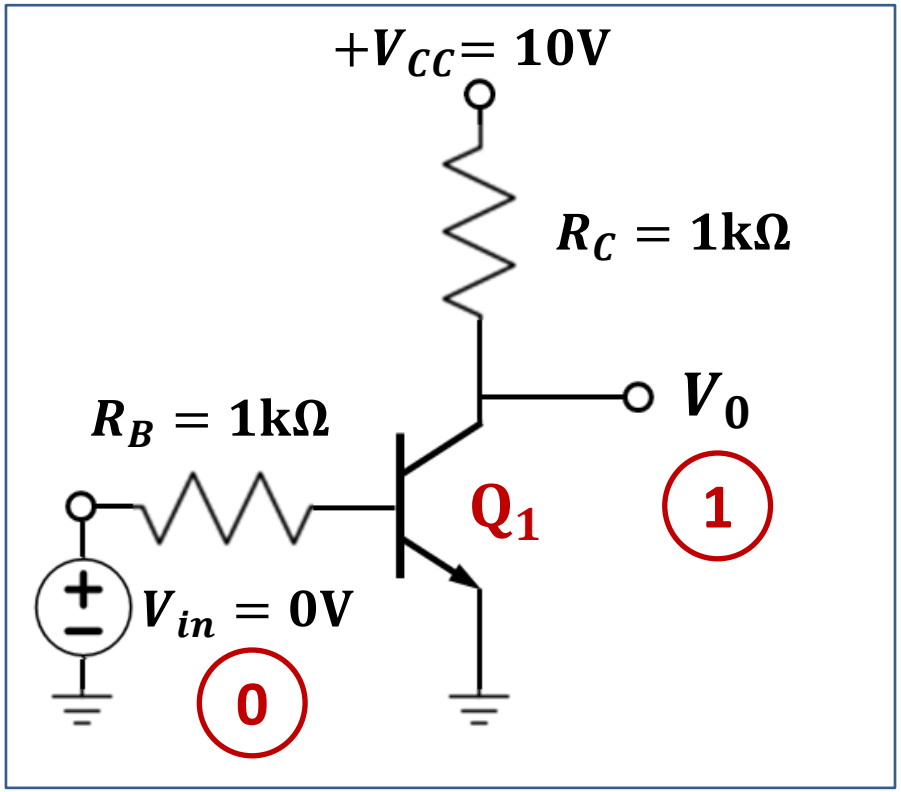
$V_{BE}(\text{ON}) = 0.7\ \text{V}$ $V_{CE}(\text{sat}) = 0.2\ \text{V}$ $\beta = 10$

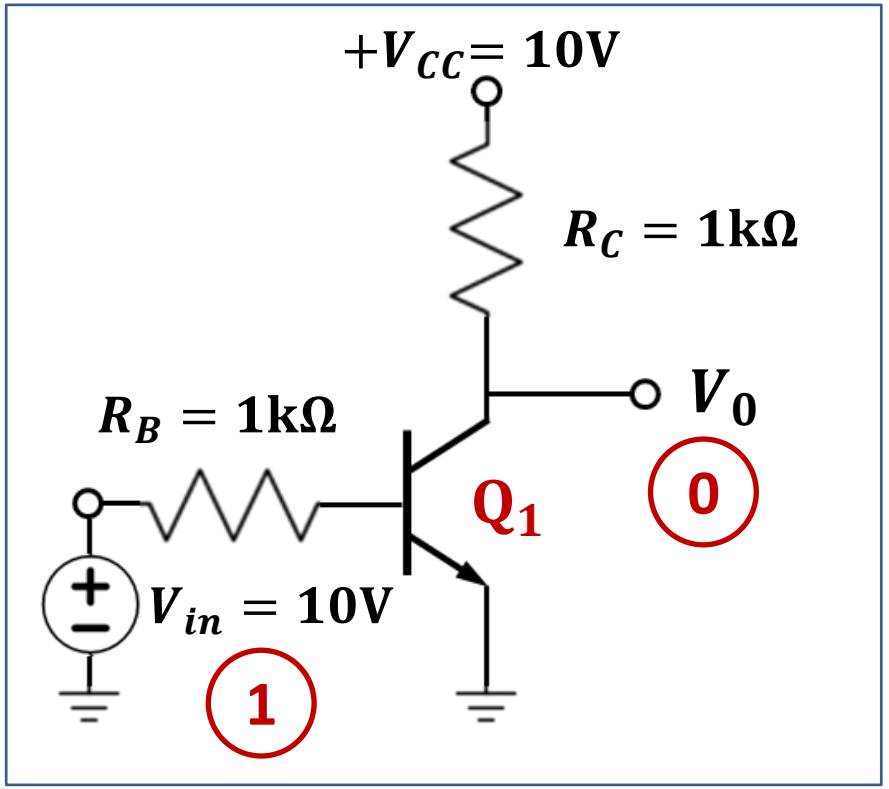


$V_0 = V_{CC} = 10\text{V}$ (1)

V_{in}	V_0
0 V (0)	10 V (1)

$V_{BE}(\text{ON}) = 0.7\ \text{V}$ $V_{CE}(\text{sat}) = 0.2\ \text{V}$ $\beta = 10$





$V_0 = V_{CC} = 10\text{V}$ (1)

V_{in}	V_0
0 V (0)	10 V (1)
10V (1)	0.2 V (0)

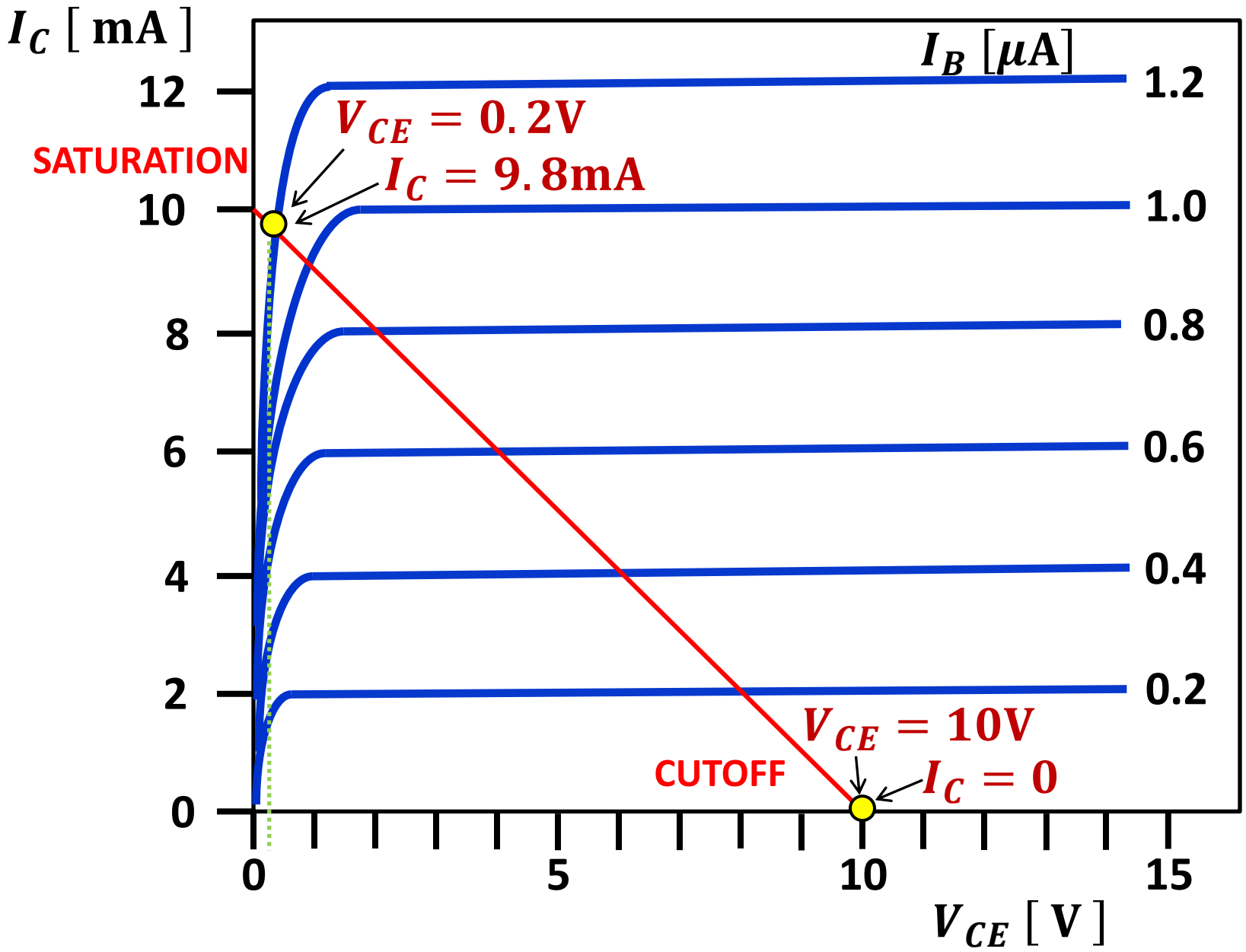
$$I_C(\text{sat}) = \frac{10 - 0.2}{1\text{k}\Omega} = 9.8\text{mA}$$

$$I_B = \frac{10 - 0.7}{1\text{k}\Omega} = 9.3\text{mA}$$

$$I_C = \beta I_B = 93\text{mA} \gg I_C(\text{sat})$$

$V_0 = 0.2\ \text{V}$ (0)

On the I-V curves



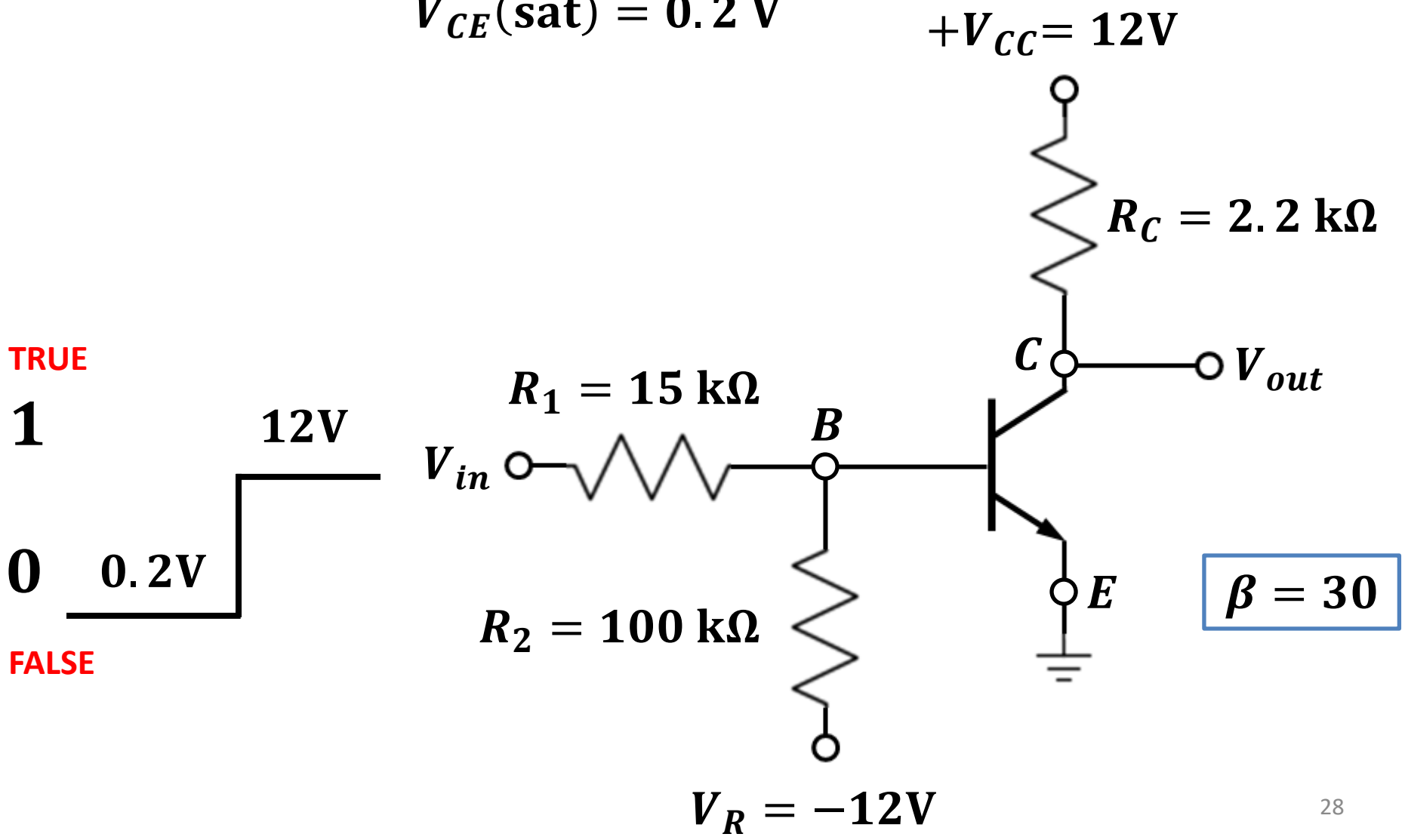
BJT inverter circuit

Another example, realized with $\pm V_{CC}$ bias

Example: Realization of inverter circuit with *n-p-n* BJT (positive logic)

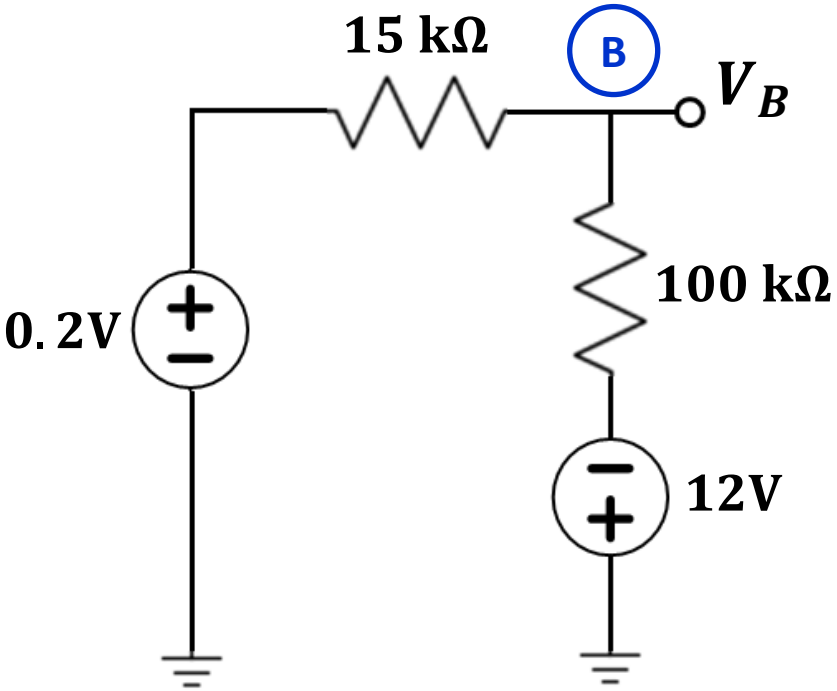
Assume $V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$



Base circuit

Node Voltage method



Input voltage $V_{in} = 0.2\ \text{V}$

Assume $I_B = 0\ \text{V}$

Thevenin equivalent source:

Node voltage at (B)

$$\frac{V_B - 0.2}{15\text{k}} + \frac{V_B - (-12)}{100\text{k}} = 0$$

$$20\text{k}\,V_B - 4\text{k} + 3\text{k}V_B + 36\text{k} = 0$$

$$V_B = -1.391\ \text{V}$$

The base *p-n* junction is OFF and as a consequence the transistor is in CUT-OFF mode. Base and collector currents are zero and

$$V_{out} = V_{CC} = 12\ \text{V}$$

Another way to solve the base circuit

Input voltage $V_{in} = 0.2\ \text{V}$

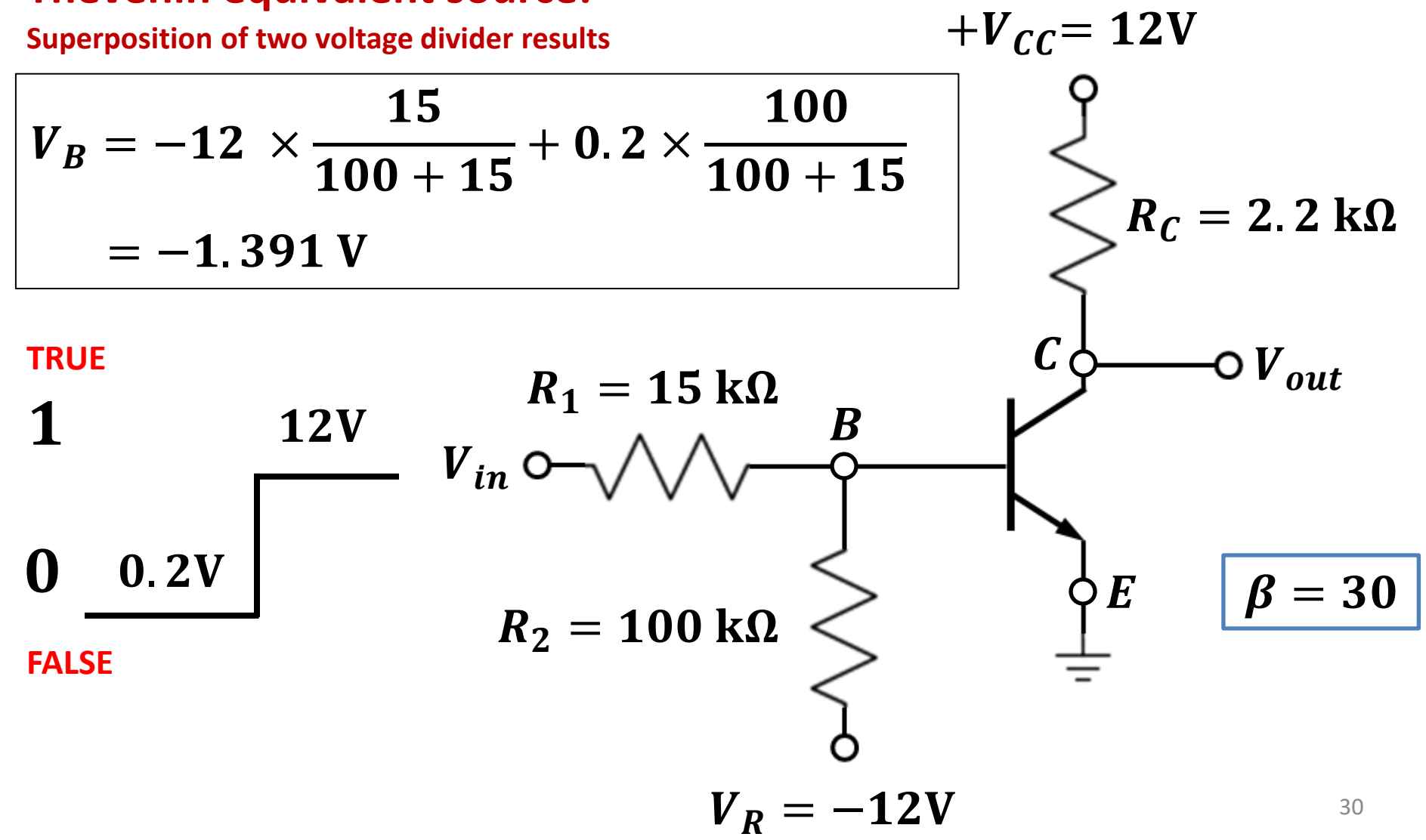
Assume $I_B = 0\ \text{V}$

Thevenin equivalent source:

Superposition of two voltage divider results

$$V_B = -12 \times \frac{15}{100+15} + 0.2 \times \frac{100}{100+15}$$

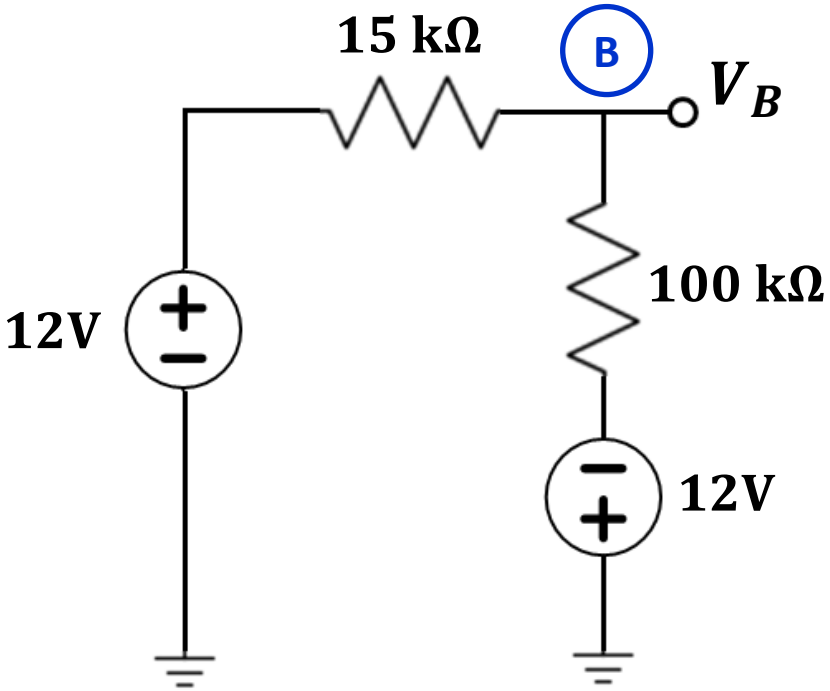
$$= -1.391\ \text{V}$$



Base circuit

Input voltage $V_{in} = 12\ \text{V}$

Thevenin equivalent source:



$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

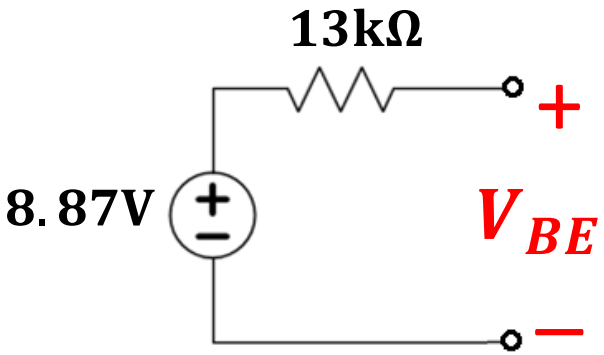
Node voltage at (B) in open circuit

$$\frac{V_B - 12}{15\text{k}} + \frac{V_B - (-12)}{100\text{k}} = 0$$

$$20\text{k}\,V_B - 240\text{k} + 3\text{k}V_B + 36\text{k} = 0$$

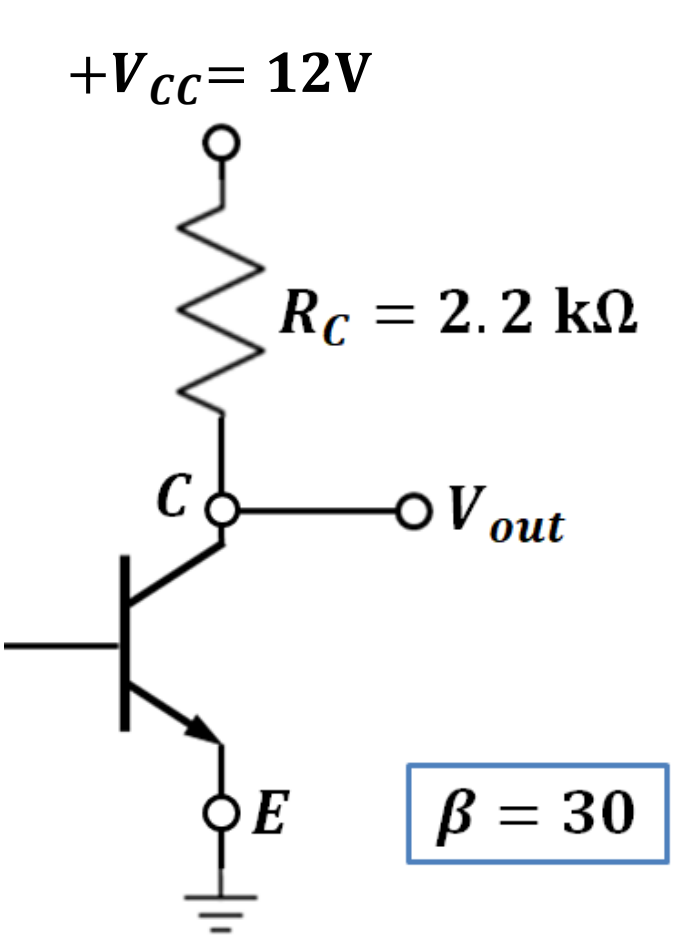
$$V_B = 8.87\ \text{V}$$

$$R_{\text{eff}} = \left(\frac{1}{15\text{k}} + \frac{1}{100\text{k}}\right)^{-1} = 13.04\text{k}\Omega$$



$$I_B = \frac{8.87 - 0.7}{13.04\ \text{k}} \approx 0.63\ \text{mA}$$

Collector circuit



$\beta = 30$

Input voltage $V_{in} = 12\ \text{V}$

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$I_B \approx 0.63\ \text{mA}$

Assuming Forward-Active mode

$I_C = \beta\, I_B = 19.9\ \text{mA}$

Check for saturation

$$I_C(\text{sat}) = \frac{V_{CC} - V_{CE}(\text{sat})}{R_C}$$

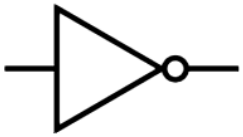
$$= \frac{11.8}{2.2\text{k}} = 5.36\ \text{mA}$$

$$I_B(\text{sat}) = I_C/\beta = 0.179\ \text{mA}$$

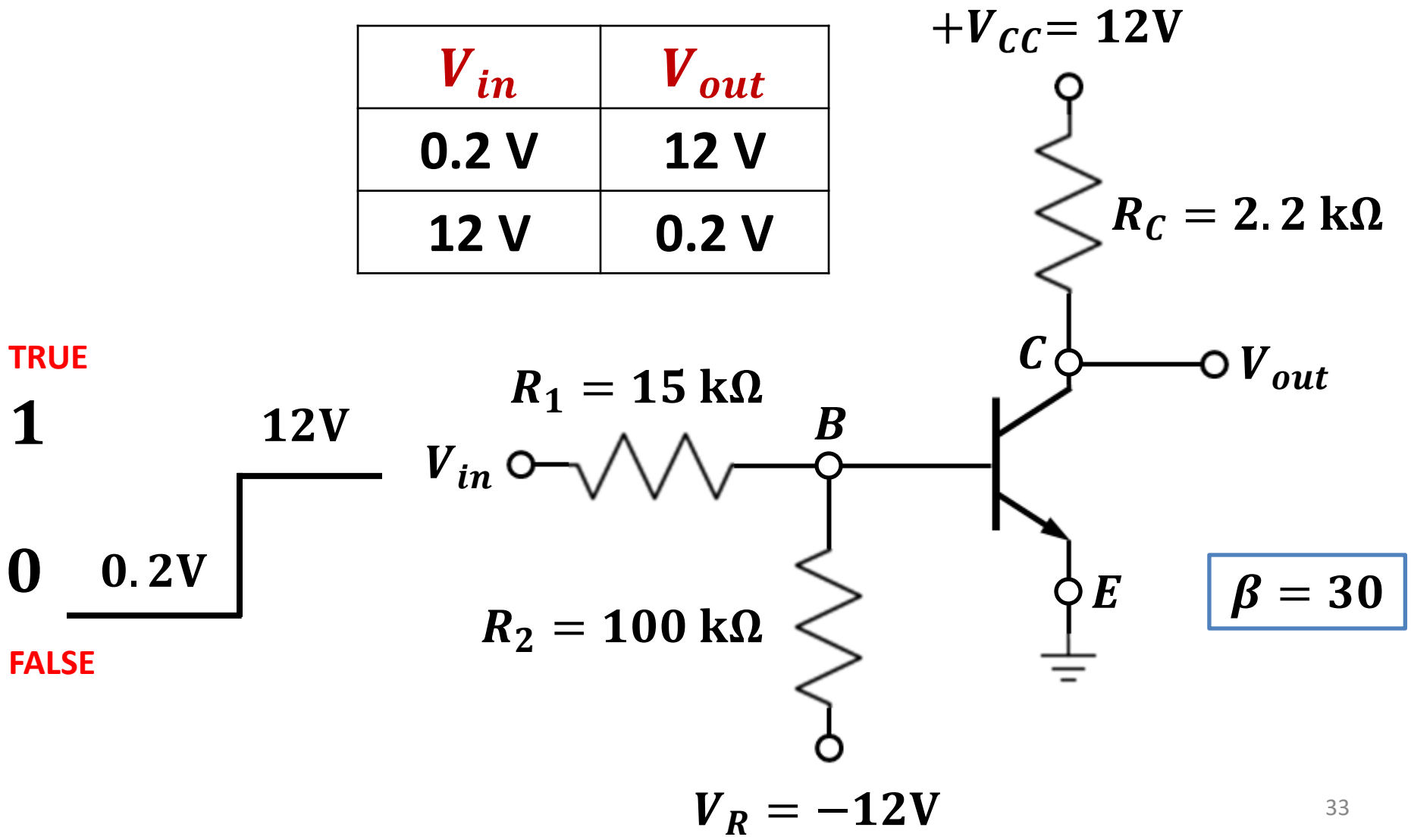
The base current exceeds the value at onset of saturation

SATURATION mode $I_C = I_C(\text{sat}) = 5.36\ \text{mA}$

Indeed, this circuit behaves like a logic inverter



V_{in}	V_{out}
0.2 V	12 V
12 V	0.2 V



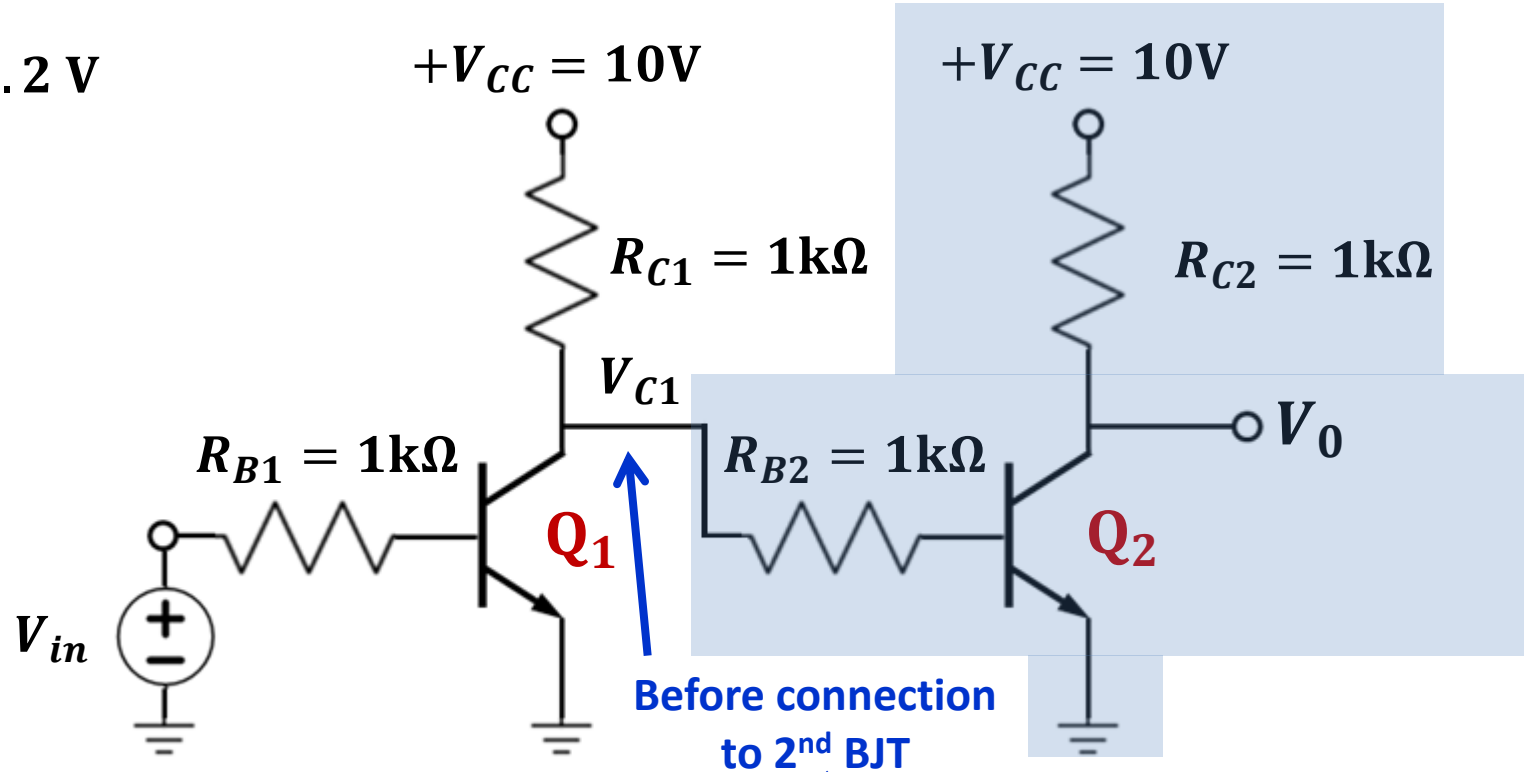
Simple logic gate design with BJT's

$V_{BE}(\mathrm{ON}) = 0.7\ \mathrm{V}$

$V_{CE}(\mathrm{sat}) = 0.2\ \mathrm{V}$

$\beta = 10$

Two BJT's in cascade



V_{in}		Q_1	V_{C1}			
0 V	0	OFF	10 V	1		
10V	1	SAT	0.2 V	0		

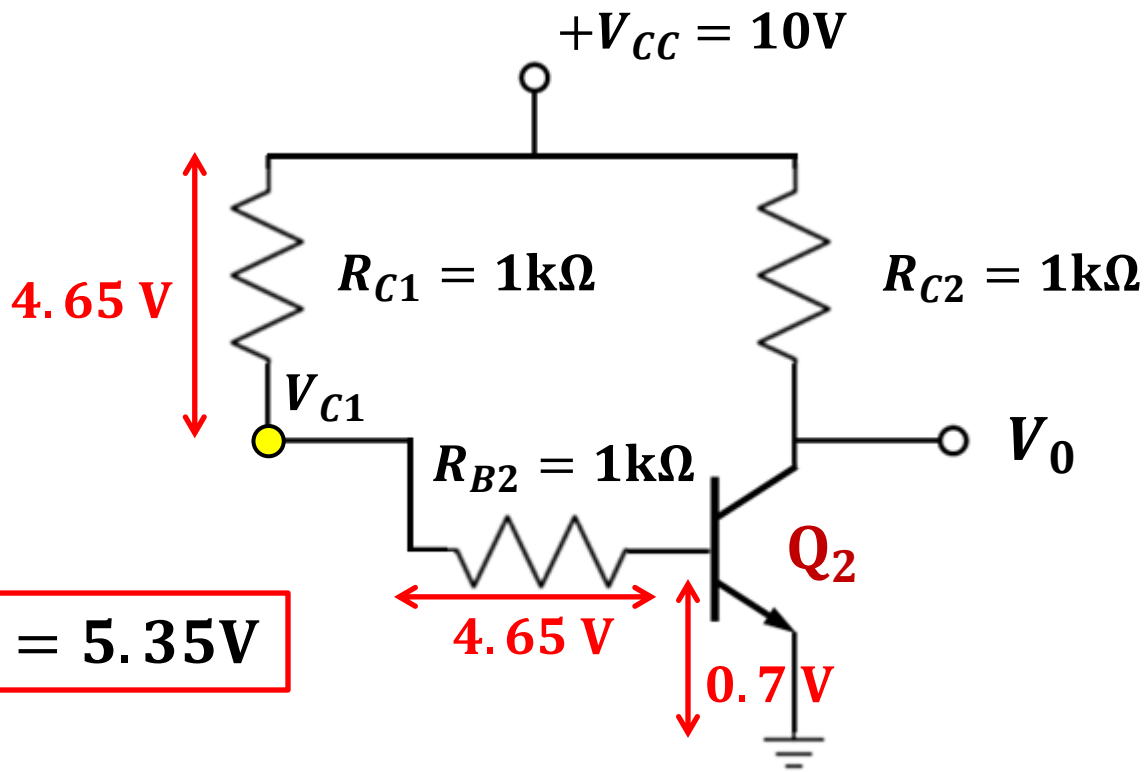
See next

Two BJT's in cascade

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$



Q_1 = OFF

$V_{C1} = 5.35\text{V}$

$$V_{CC} - (R_{C1} + R_{B2})I_{B2} - V_{BE}(\text{ON}) = 0$$

$$10 - 2\text{k}\Omega\, I_{B2} - 0.7 = 0$$

$$I_{B2} = 9.3/2\text{k} = 4.65\text{mA}$$

Assuming forward-active mode

$$I_{C2} = 46.5\text{mA}$$

$$I_{C2}(\text{sat}) = \frac{10 - 0.2}{1\text{k}} = 9.8\text{mA}$$

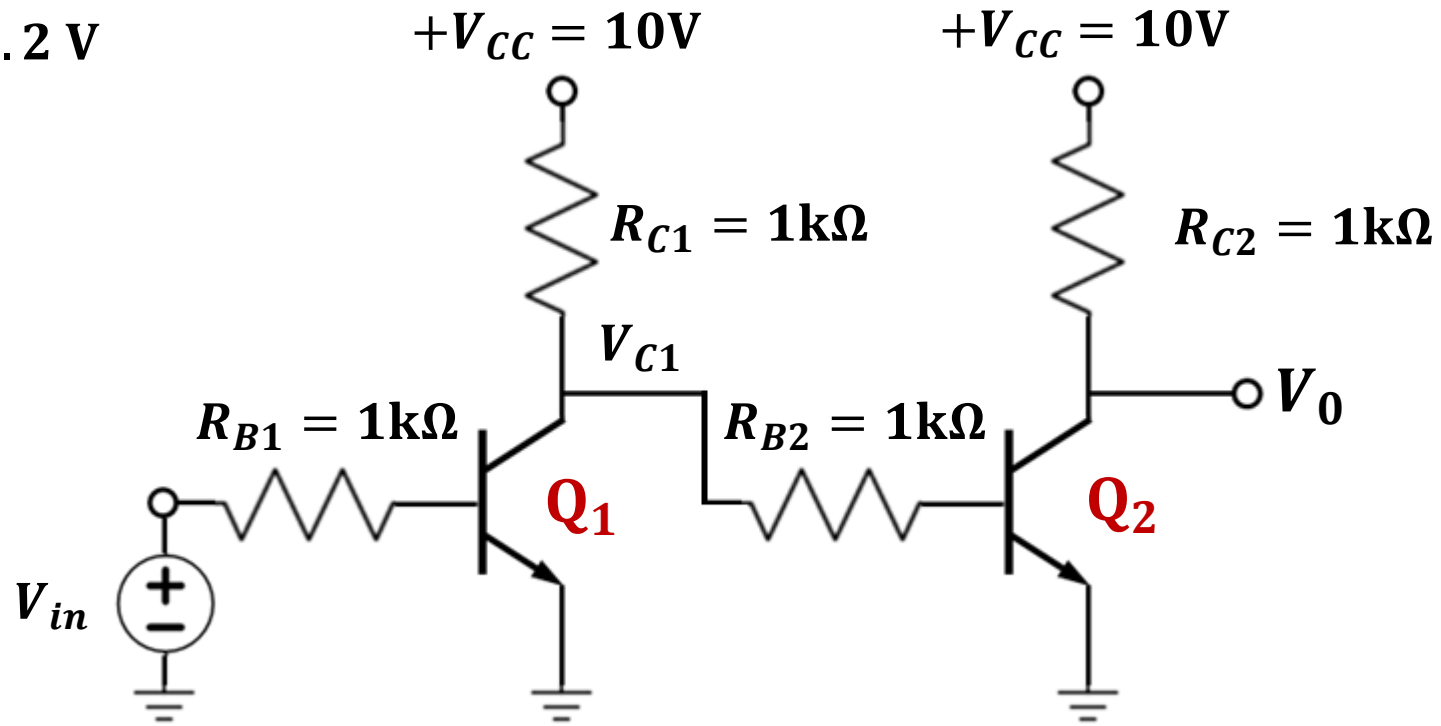
Q_2 = SATURATION

$V_{BE}(\mathrm{ON}) = 0.7\ \mathrm{V}$

$V_{CE}(\mathrm{sat}) = 0.2\ \mathrm{V}$

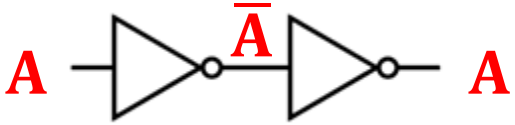
$\beta = 10$

Two BJT's in cascade



V_{in}	Q_1	V_{C1}	Q_2	V_0
0 V (0)	OFF	5.35V (1)	SAT	0.2 V (0)
10V (1)	SAT	0.2 V (0)	OFF	10 V (1)

Two NOT gates in series



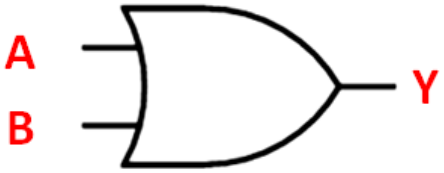
OR Logic Gate

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

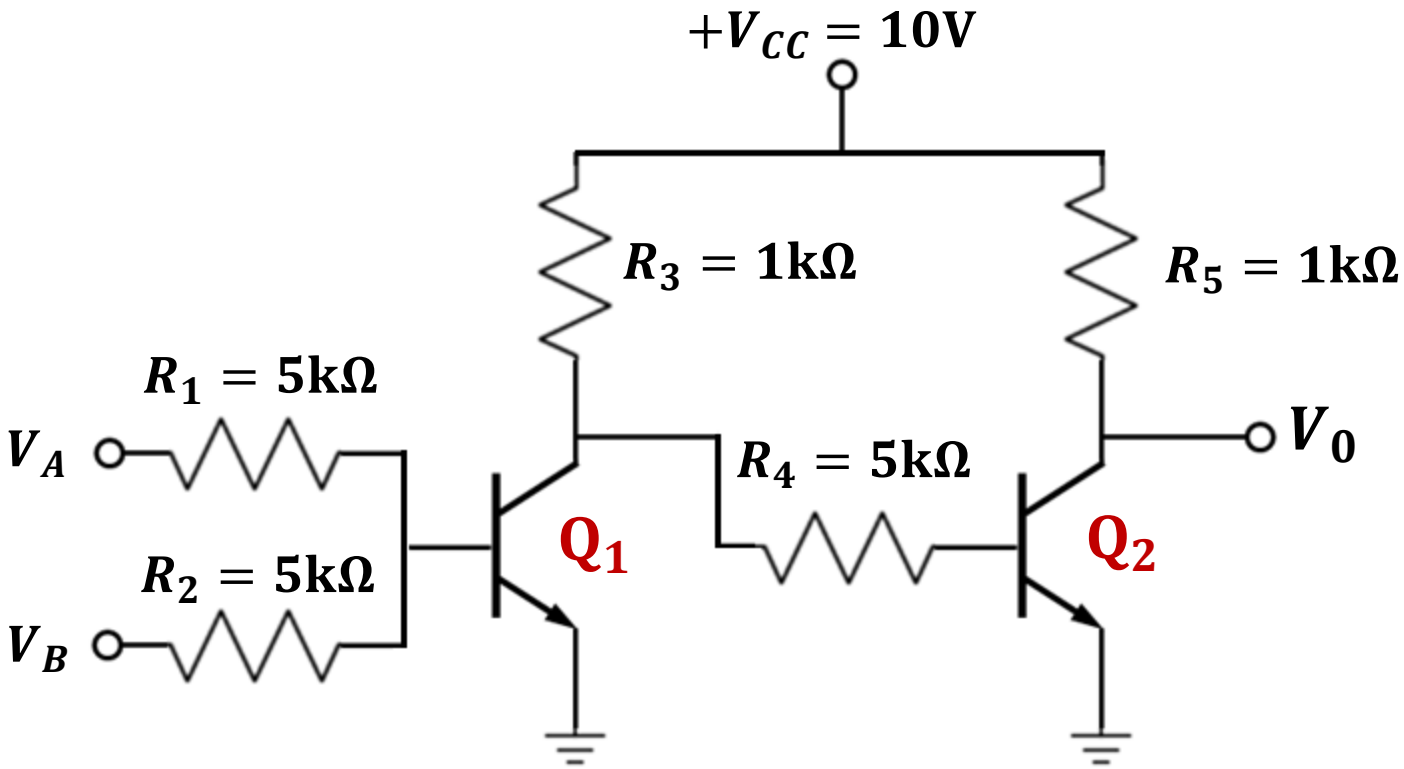
$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$

OR



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

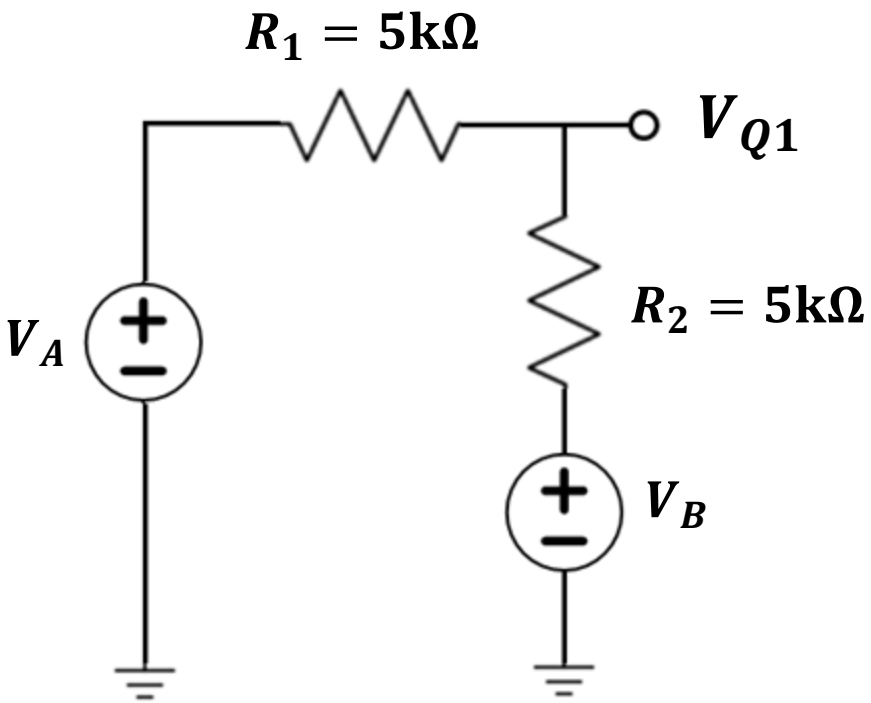


OR Logic Gate

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$



$$\frac{V_{Q1} - V_A}{5\text{k}} + \frac{V_{Q1} - V_B}{5\text{k}} = 0$$

$$V_{Q1} = \frac{V_A + V_B}{2}$$

$V_A = 0 \qquad V_B = 0$

$V_{Q1} = 0$

$V_A = 10\text{V} \qquad V_B = 0$

$V_{Q1} = 5\text{V}$

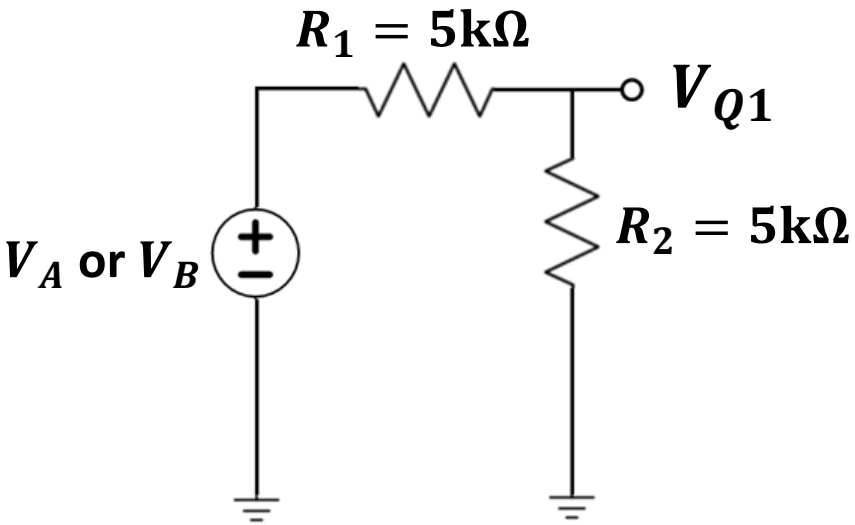
$V_A = 0 \qquad V_B = 10\text{V}$

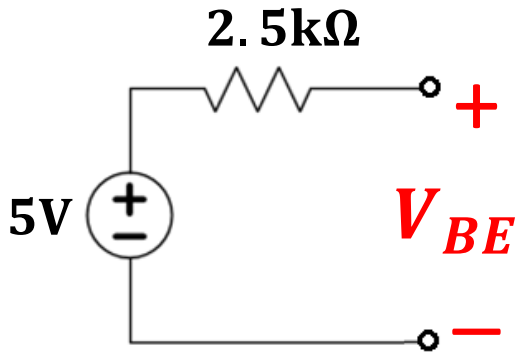
$V_{Q1} = 5\text{V}$

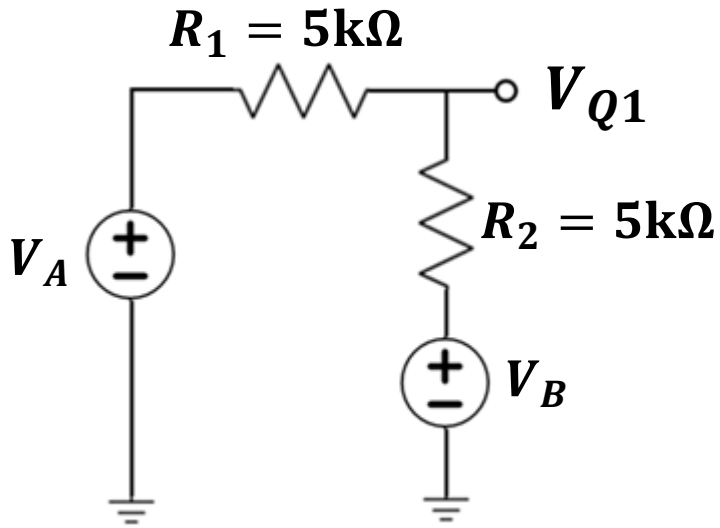
$V_A = 10\text{V} \qquad V_B = 10\text{V}$

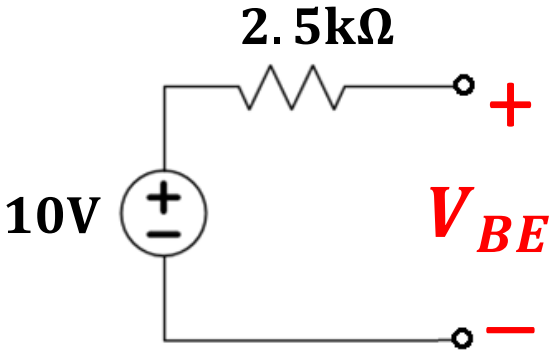
$V_{Q1} = 10\text{V}$

Equivalent base circuit for Q_1







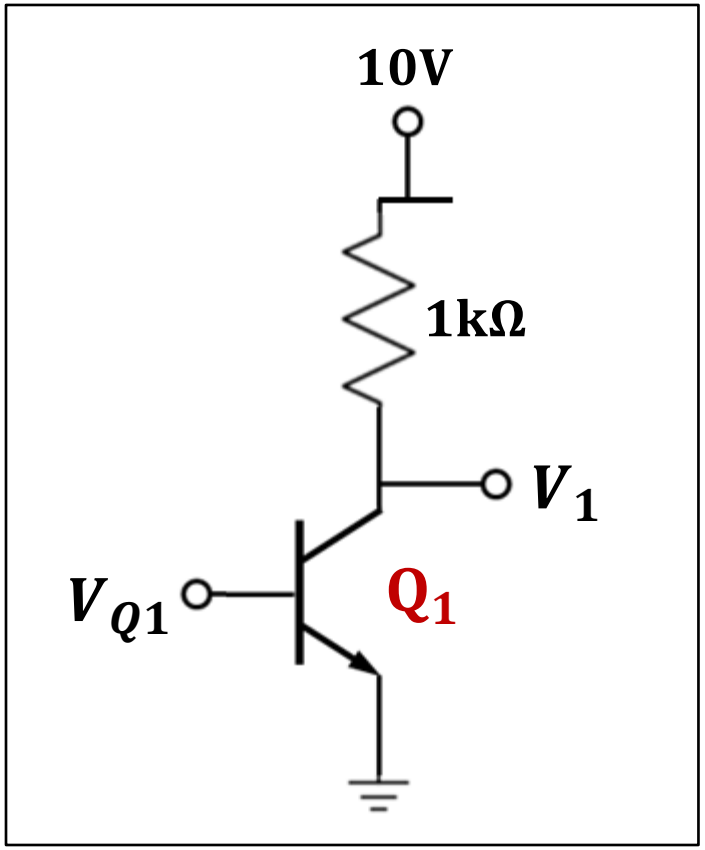


OR Logic Gate

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$



$$I_C(\text{sat}) = \frac{10 - 0.2}{1\text{k}\Omega} = 9.8\text{mA}$$

$V_{Q1} = 0$

$$V_1 = 10\ \text{V}$$

$V_{Q1} = 5\text{V}$

$$I_B = \frac{5 - 0.7}{2.5\text{k}\Omega} = 1.72\text{mA}$$

$$I_C = \beta I_B = 17.2\text{mA} \gg I_C(\text{sat})$$

$$V_1 = 0.2\ \text{V}$$

$V_{Q1} = 10\text{V}$

$$I_B = \frac{10 - 0.7}{2.5\text{k}\Omega} = 3.72\text{mA}$$

$$I_C = \beta I_B = 37.2\text{mA} \gg I_C(\text{sat})$$

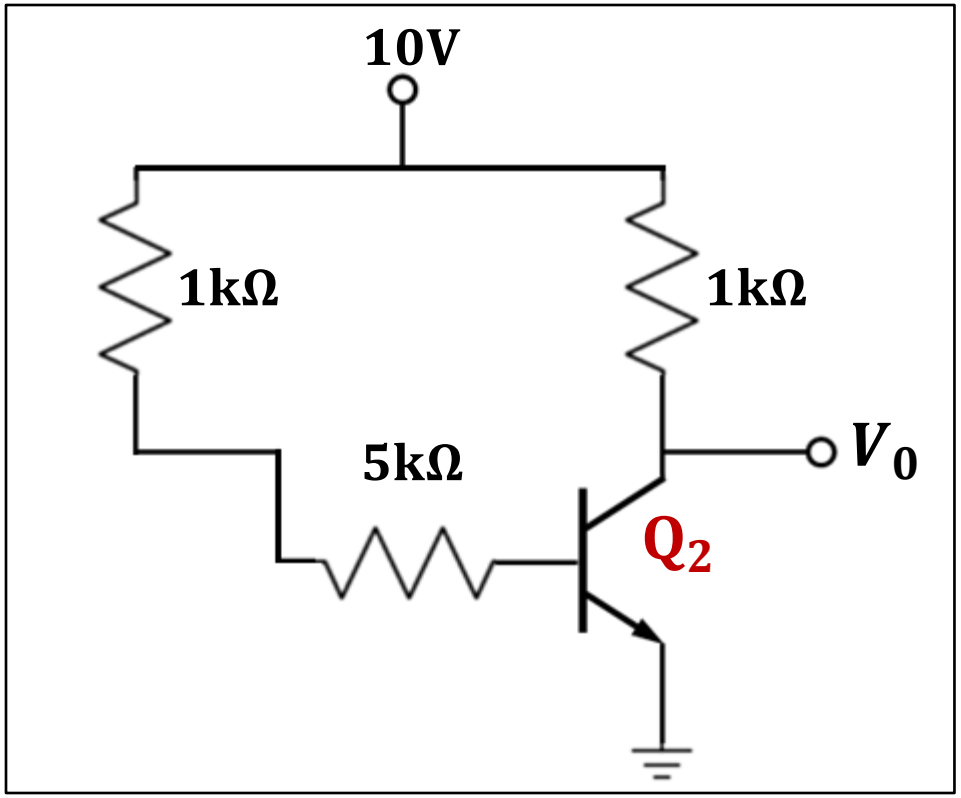
$$V_1 = 0.2\ \text{V}$$

OR Logic Gate

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$



$$I_C(\text{sat}) = \frac{10 - 0.2}{1\text{k}\Omega} = 9.8\text{mA}$$

Q_1 OFF

$$I_B = \frac{10 - 0.7}{1\text{k}\Omega + 5\text{k}\Omega} = 1.55\text{mA}$$

$$I_C = \beta I_B = 15.5\text{mA} \gg I_C(\text{sat})$$

$$V_0 = 0.2\ \text{V}$$

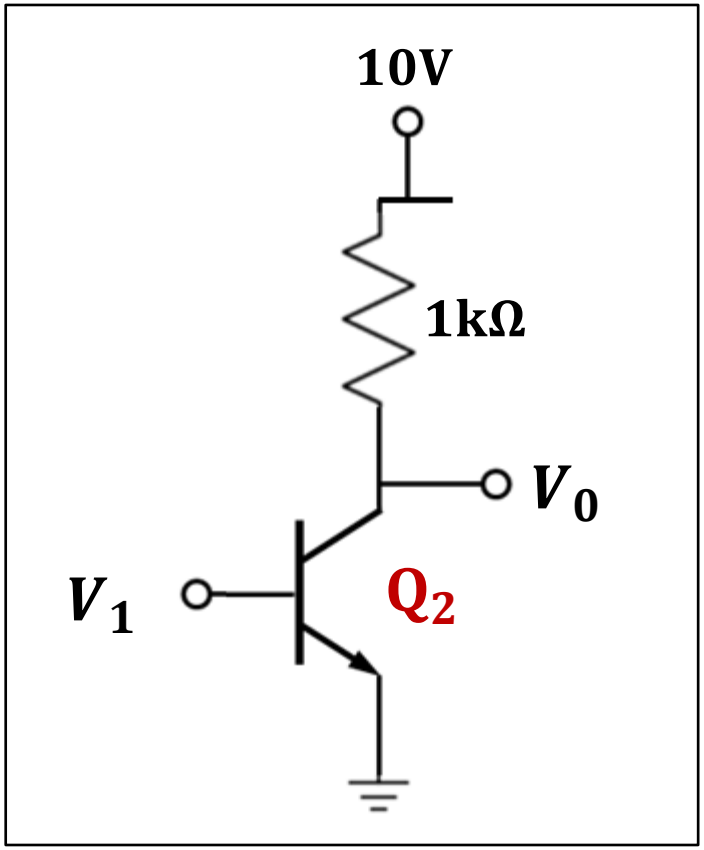
Q_2 SATURATION

OR Logic Gate

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$



Q_1 SATURATION

$V_1 = V_{CE}(\text{sat})$

$= 0.2\text{V} < V_{BE}(\text{ON})$

$I_B = 0$

$I_C = 0$

$V_0 = 10\ \text{V}$

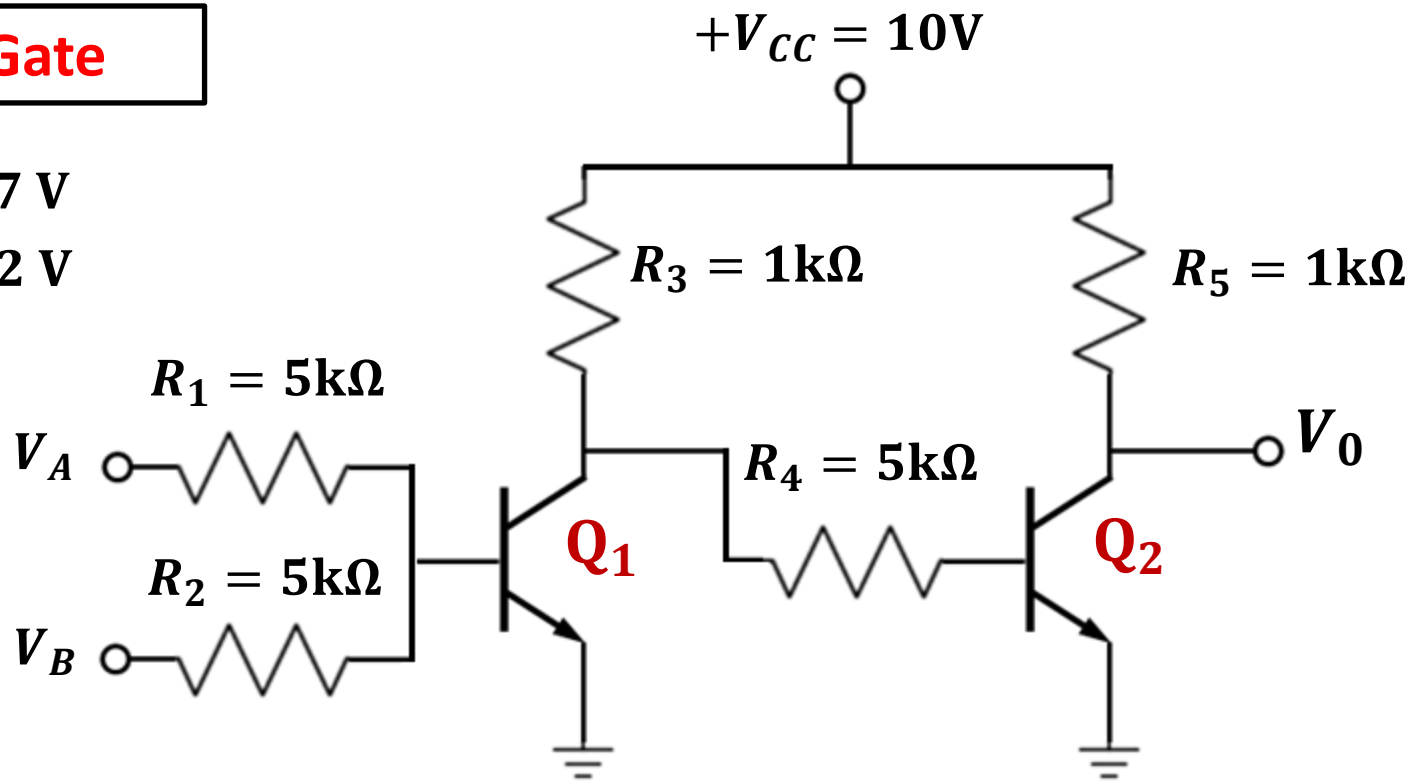
Q_2 OFF

OR Logic Gate

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$



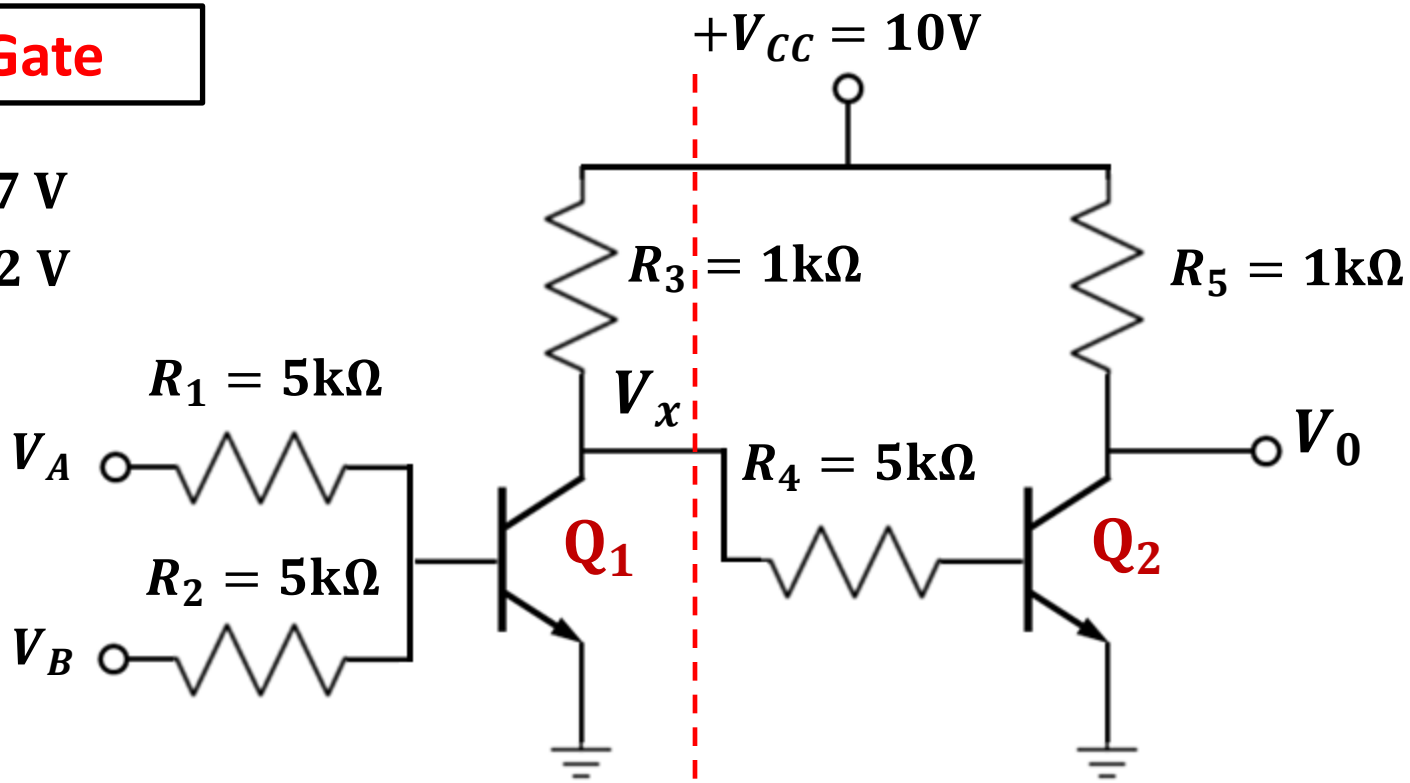
V_A		V_B		Q_1	Q_2	V_0	
0V	0	0V	0	OFF	SAT	0.2 V	0
0V	0	10V	1	SAT	OFF	10 V	1
10V	1	0V	0	SAT	OFF	10V	1
10V	1	10V	1	SAT	OFF	10V	1

OR Logic Gate

$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$

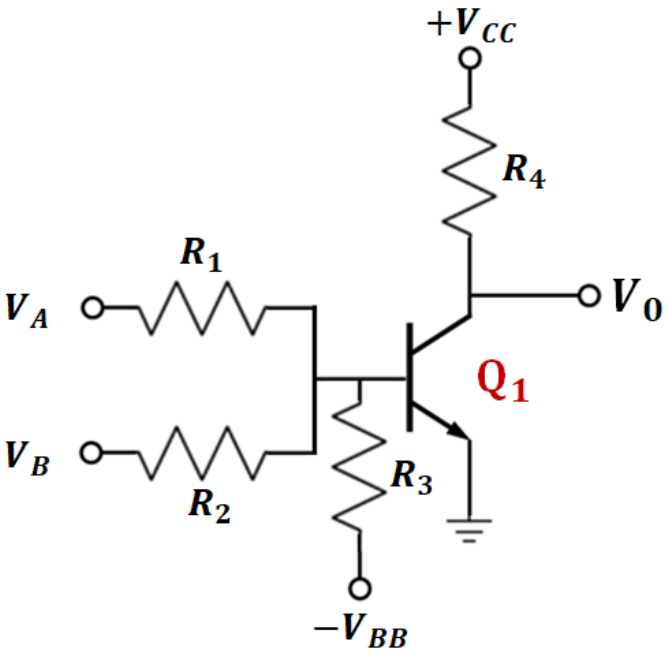


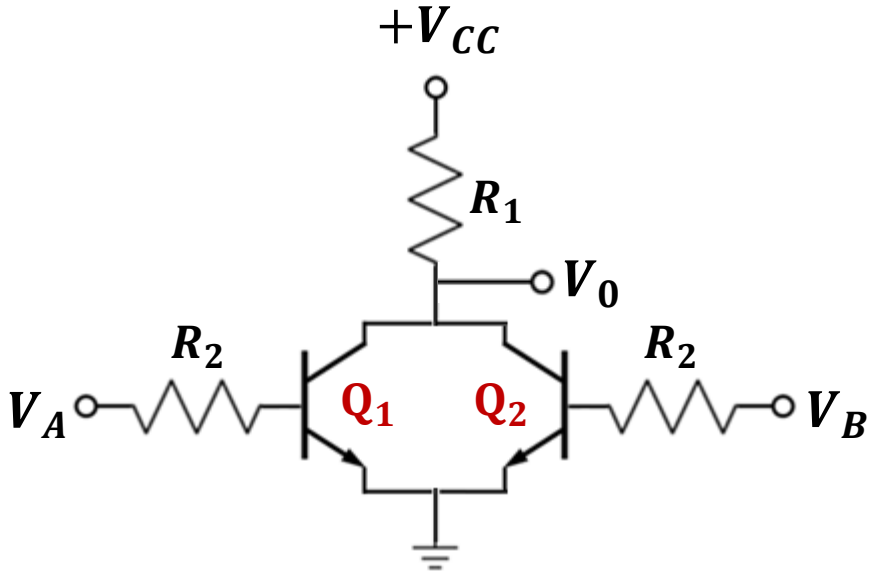
V_A		V_B		Q_1	V_x	
0V	0	0V	0	OFF	10V	1
0V	0	10V	1	SAT	0.2V	0
10V	1	0V	0	SAT	0.2V	0
10V	1	10V	1	SAT	0.2V	0

After connection to Q_2

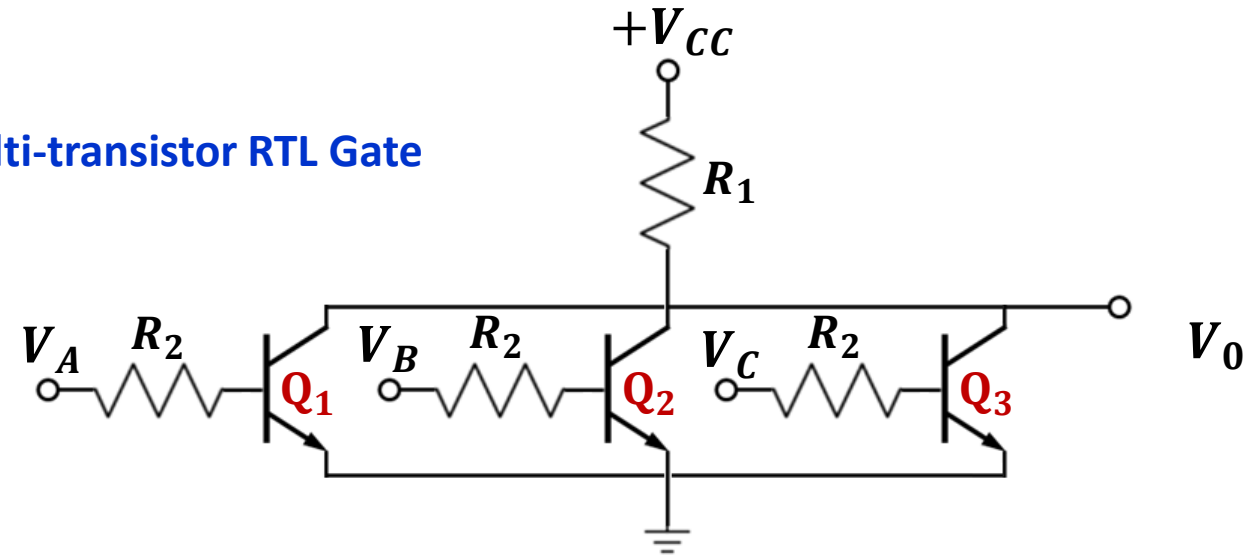
$$V_x = 7.75\ \text{V}$$

Other NOR implementations



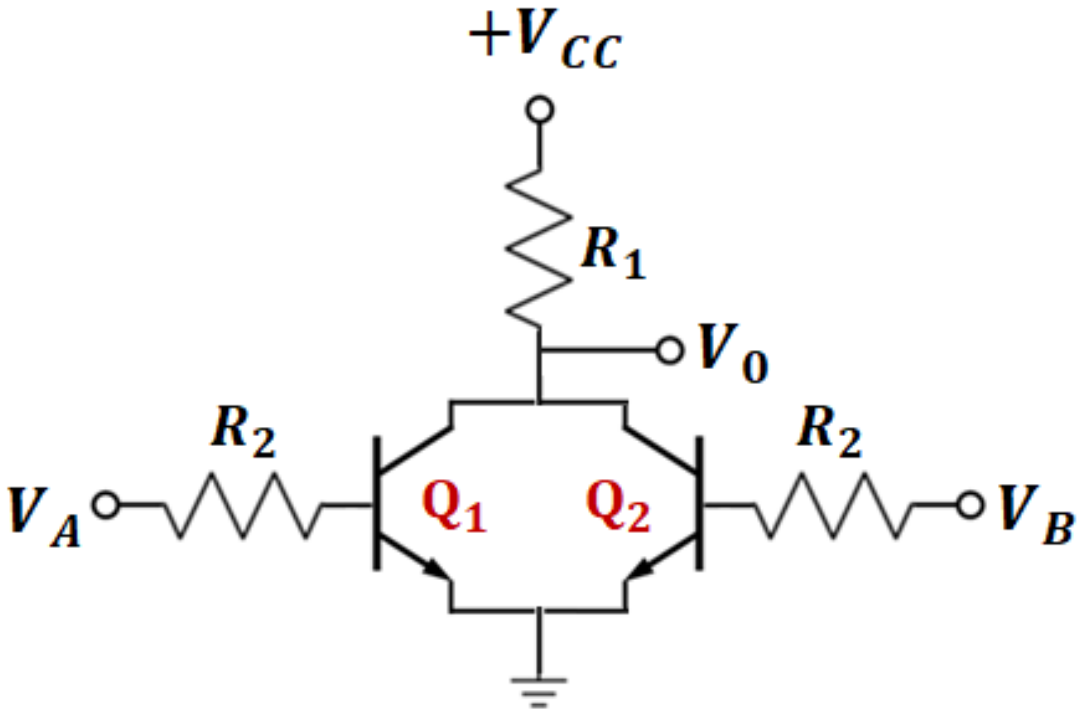


Multi-transistor RTL Gate



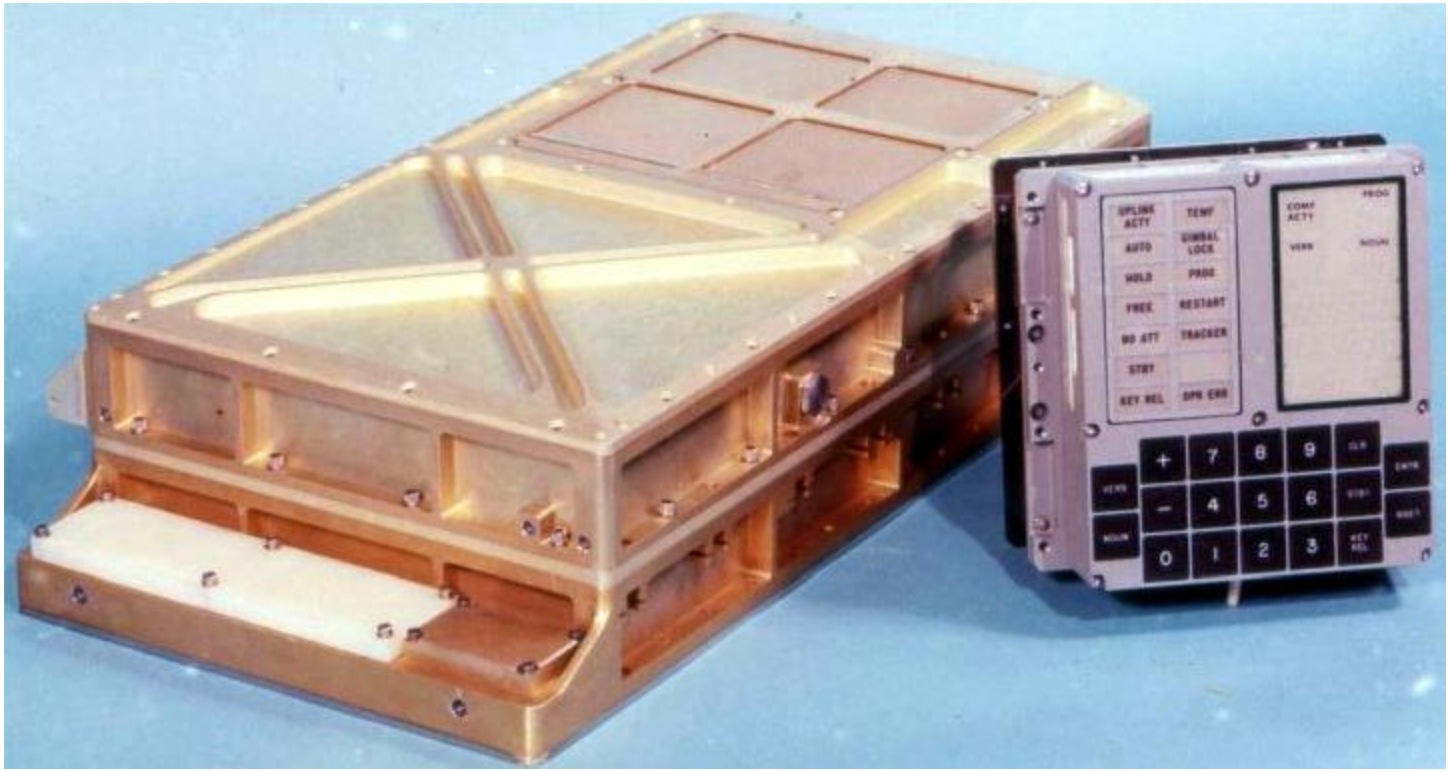
NOR

$V_{CC} = 10V$

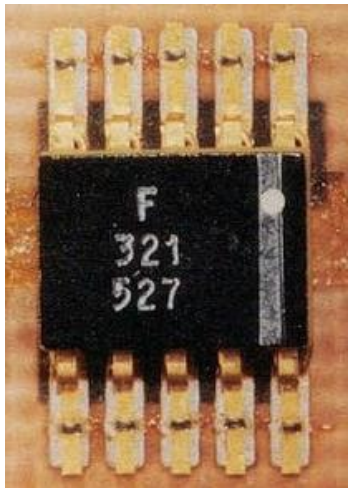


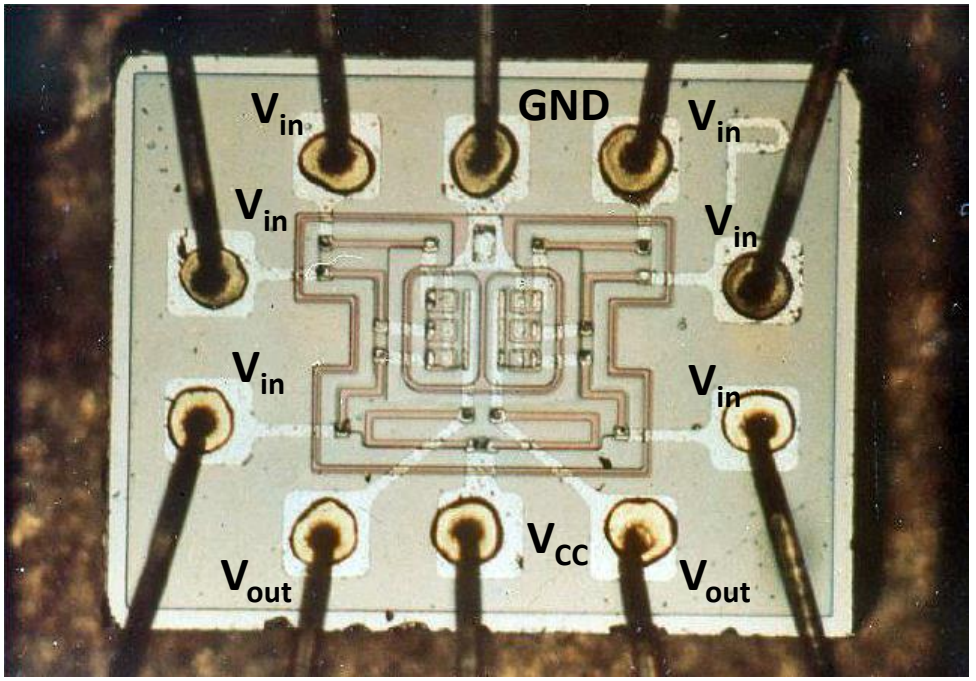
V_A	V_B	Q_1	Q_2	V_0
0V (0)	0V (0)	OFF	OFF	10 V (1)
0V (0)	10V (1)	OFF	SAT	0.2 V (0)
10V (1)	0V (0)	SAT	OFF	0.2 V (0)
10V (1)	10V (1)	SAT	SAT	0.2 V (0)

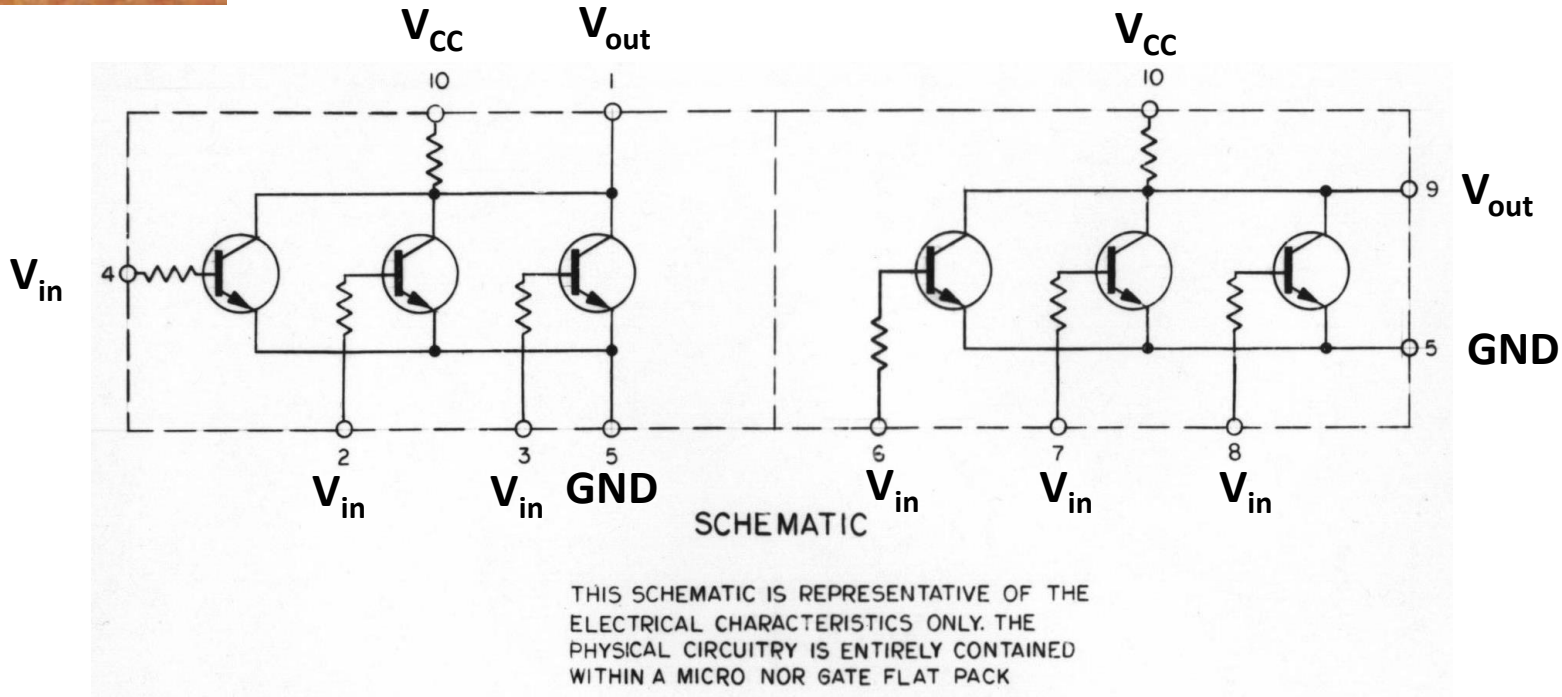
RTL-based NOR circuits were used in the Apollo Guidance Computer that went to the moon (the first computer using silicon integrated circuits)

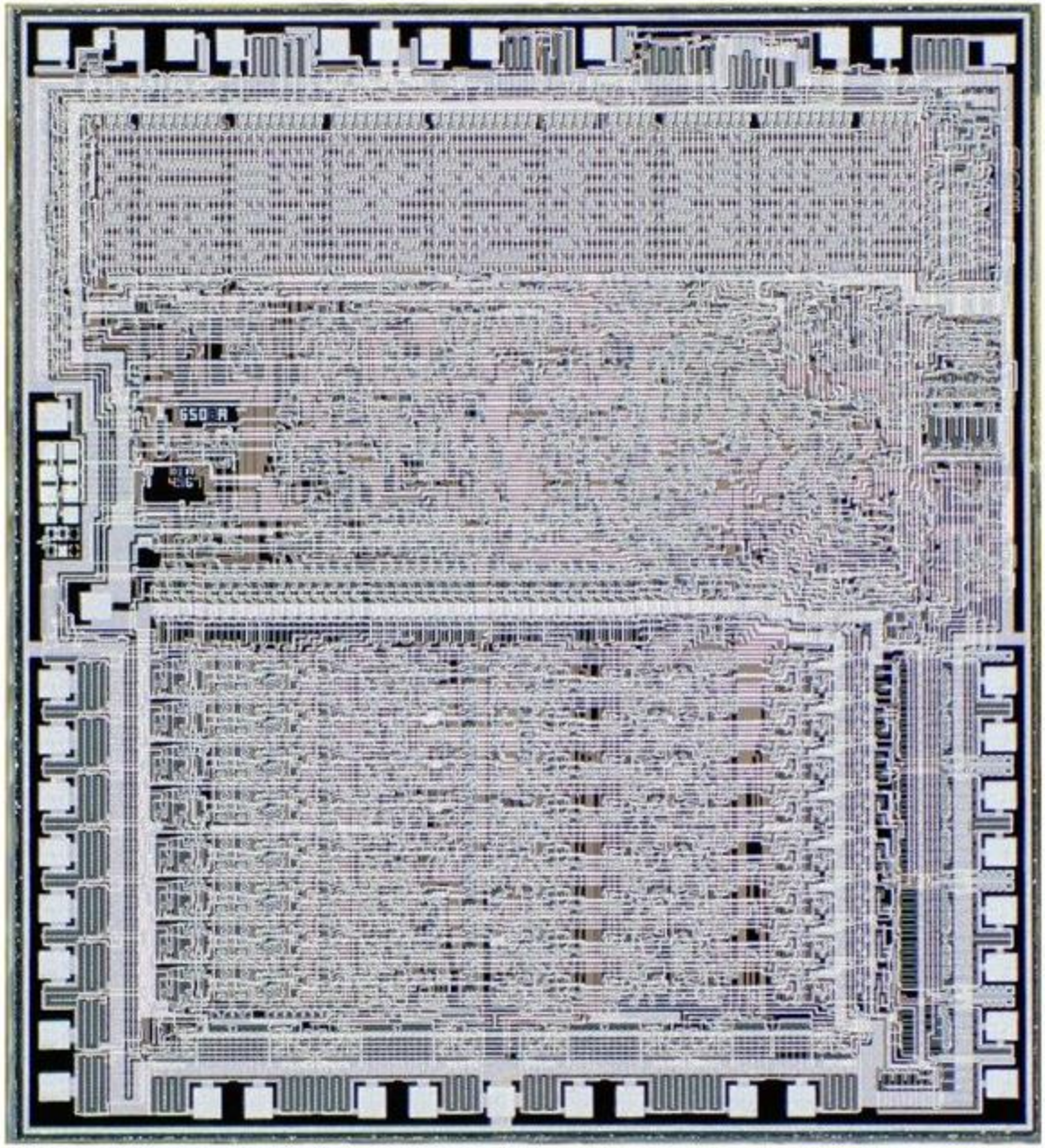


Silicon integrated circuit with two 3-inputs NOR gates, used in the Apollo Guidance computer.









MOS Technology
6502 8-bit microprocessor (1975)
3510 transistors (MOSFET)

CPU of:
- **Apple II**
- **Atari 400 & 800**
- **BBC Micro**
- **Commodore PET & VIC-20**

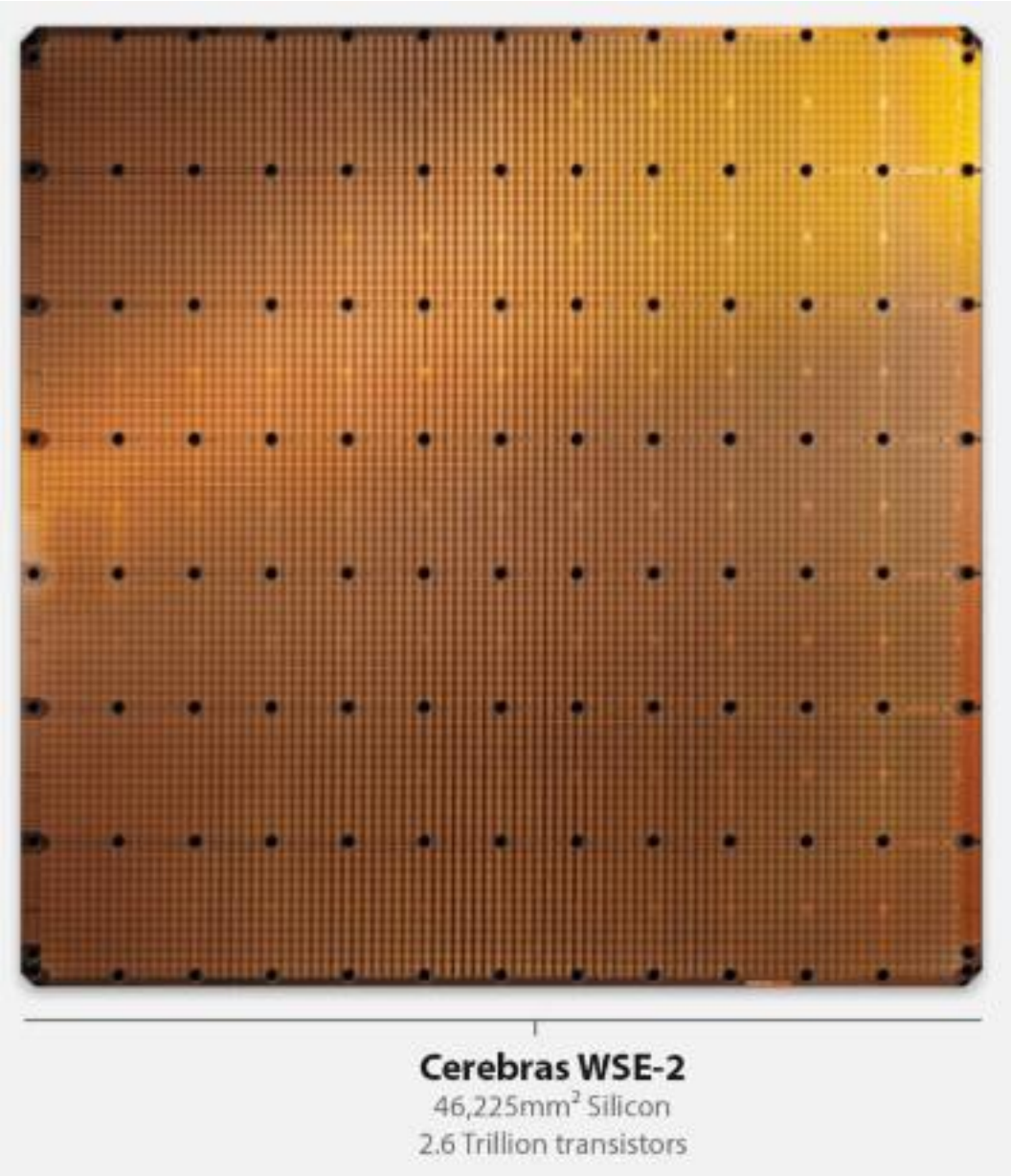
Photo: © Antoine Bercovici

Semiconductor chips in consumer products have billions of transistors

Apple M2 Max has 67 billion MOSFETs (2023)
Apple M2 Ultra (2×M2 Max) has 134 billion MOSFETs

AMD's MI300X has 153 billion MOSFETs (2023)

The Wafer Scale Engine 2 (WS2) deep-learning processor by Cerebras has 2.6 trillion MOSFETs



850,000 cores

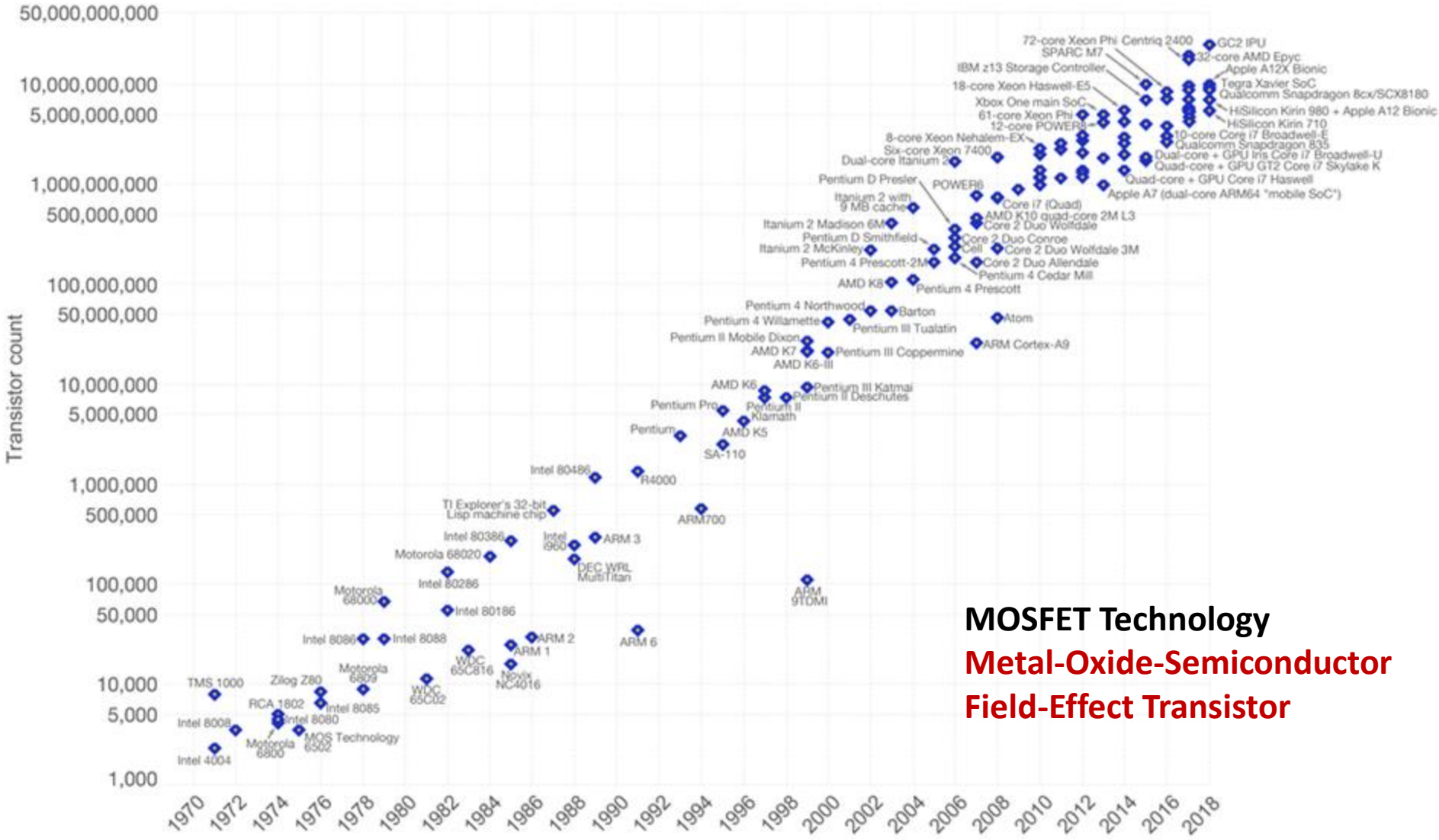
Memory bandwidth = 20 Petabytes/sec

https://www.cerebras.net/product-chip/

Moore's Law – The number of transistors on integrated circuit chips (1971-2018)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are linked to Moore's law.

Our World in Data



MOSFET Technology

Metal-Oxide-Semiconductor Field-Effect Transistor

The data visualization is available at OurWorldinData.org.

- **Estimated number of grains of sand on Earth**

$\approx 7.5 \times 10^{18}$ (seven quintillion five hundred quadrillions grains)

- **Estimated number of transistors fabricated since 1947**

$\approx 2.9 \times 10^{21}$ (2.0 sextillion transistors) **[2014]**

$\approx 1.3 \times 10^{22}$ (13 sextillion transistors) **[2022]**

- **Estimated number of stars in the Universe visible with the Hubble telescope (2003)**
- **Estimated number of H_{2O} molecules in 10 drops of water**

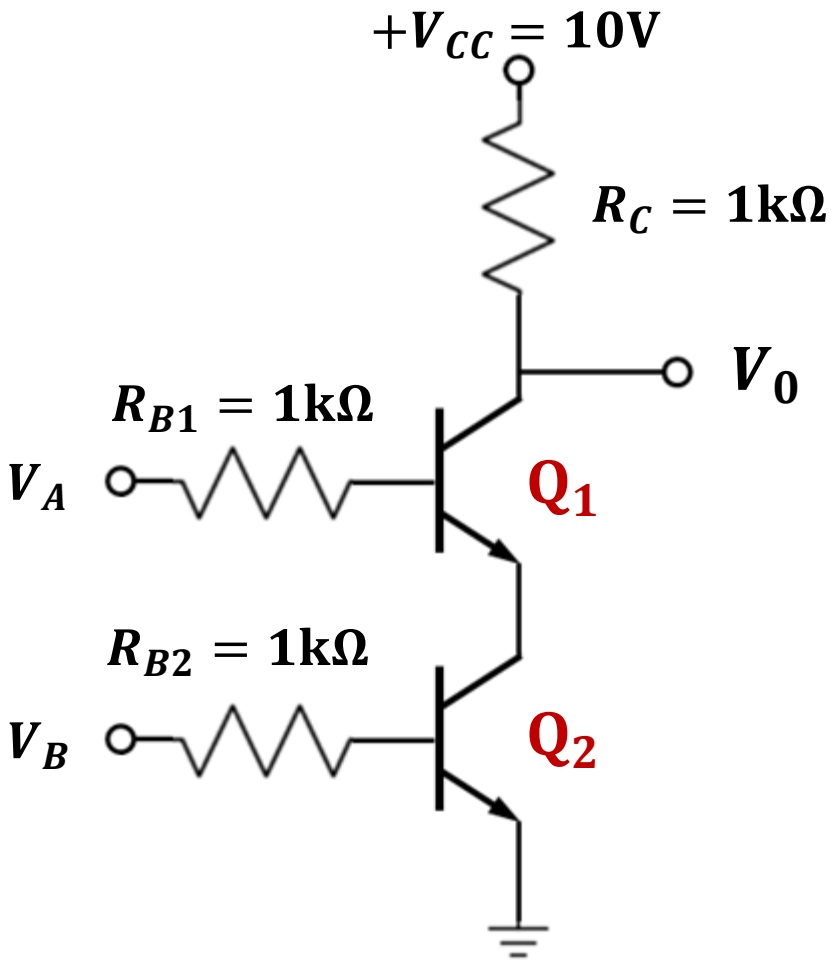
$\approx 7.0 \times 10^{22}$ (70 sextillions)

Two transistors in series

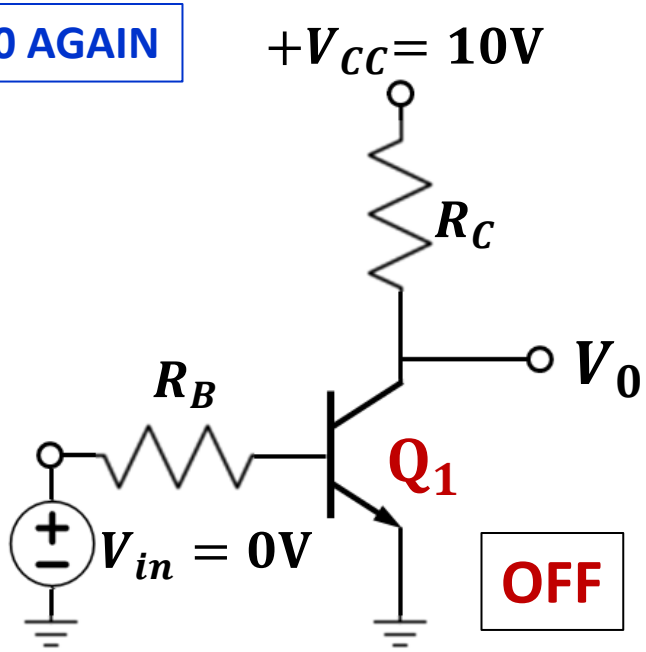
$V_{BE}(\mathrm{ON}) = 0.7\ \mathrm{V}$

$V_{CE}(\mathrm{sat}) = 0.2\ \mathrm{V}$

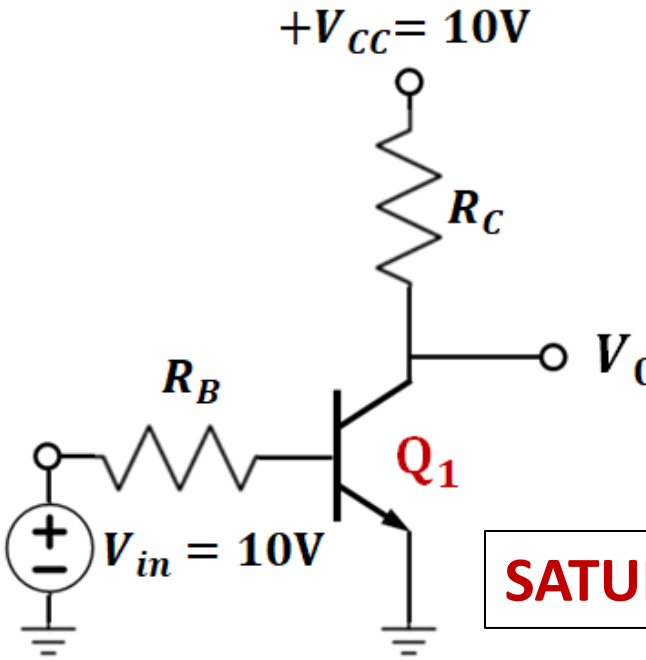
$\beta = 10$



SLIDE #20 AGAIN

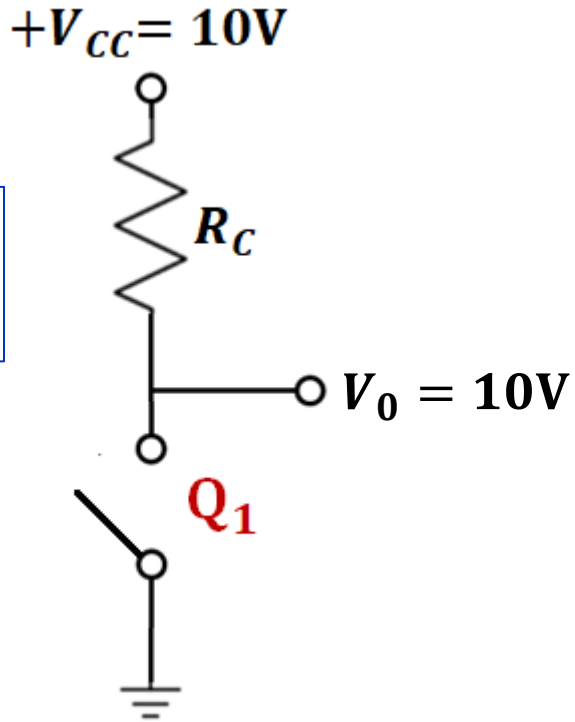


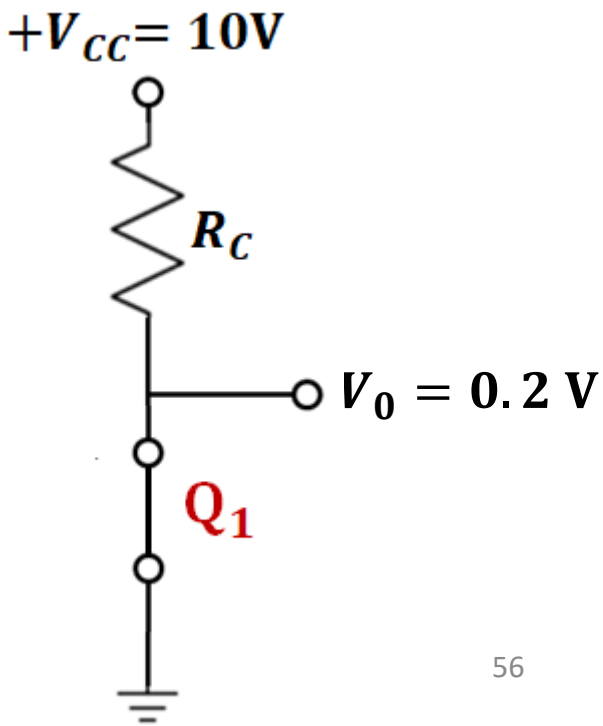
OFF



SATURATION

Transistors are like switches





Two transistors in series

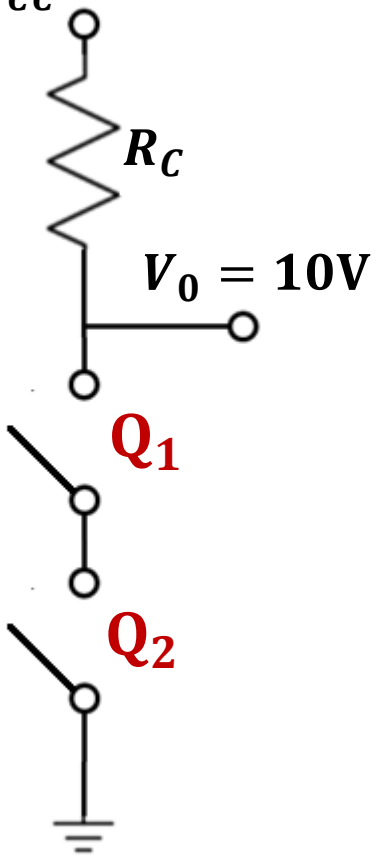
$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$

$V_A = V_B = 0\text{V}$

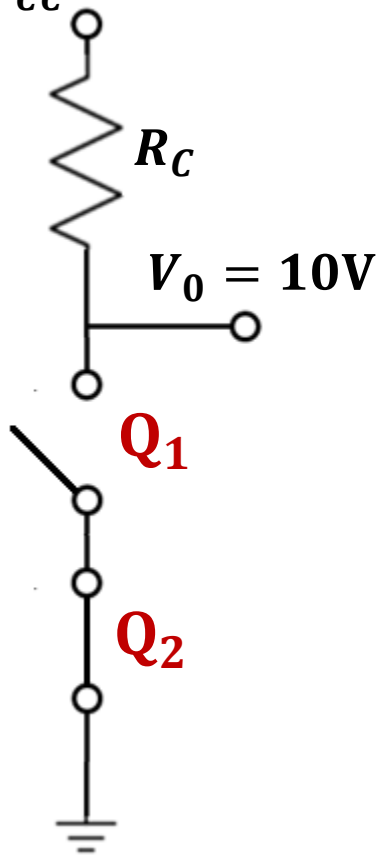
$+V_{CC} = 10\text{V}$



$V_A = 0\text{V}$

$V_B = 10\text{V}$

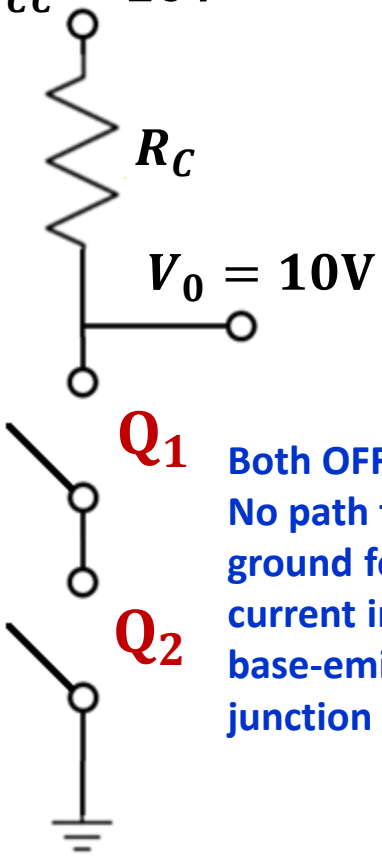
$+V_{CC} = 10\text{V}$



$V_A = 10\text{V}$

$V_B = 0\text{V}$

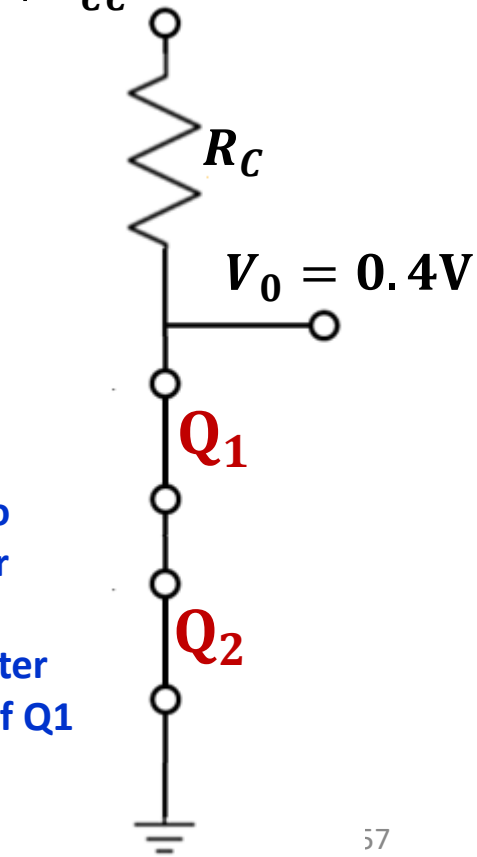
$+V_{CC} = 10\text{V}$



Both OFF
No path to ground for current in base-emitter junction of Q1

$V_A = V_B = 10\text{V}$

$+V_{CC} = 10\text{V}$



Two transistors in series

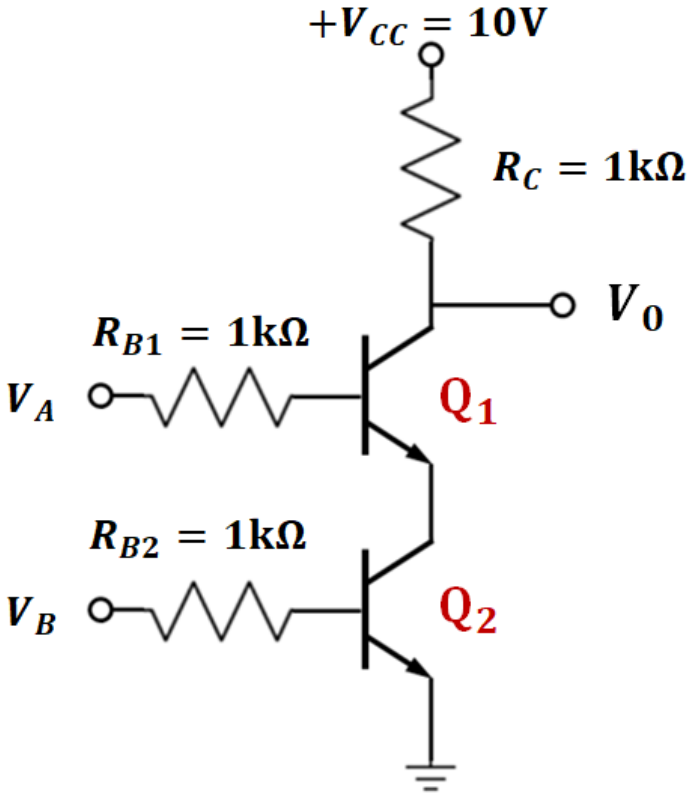
$V_{BE}(\text{ON}) = 0.7\ \text{V}$

$V_{CE}(\text{sat}) = 0.2\ \text{V}$

$\beta = 10$

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

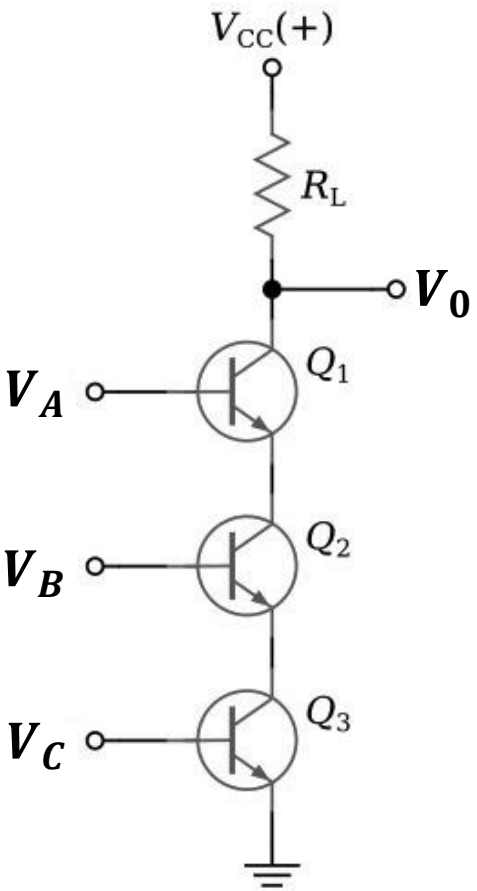


V_A	V_B	Q_1	Q_2	V_0
0V (0)	0V (0)	OFF	OFF	10 V (1)
0V (0)	10V (1)	OFF	SAT	10 V (1)
10V (1)	0V (0)	OFF	OFF	10V (1)
10V (1)	10V (1)	SAT	SAT	0.4V (0)

NAND implementation with other BJT technologies

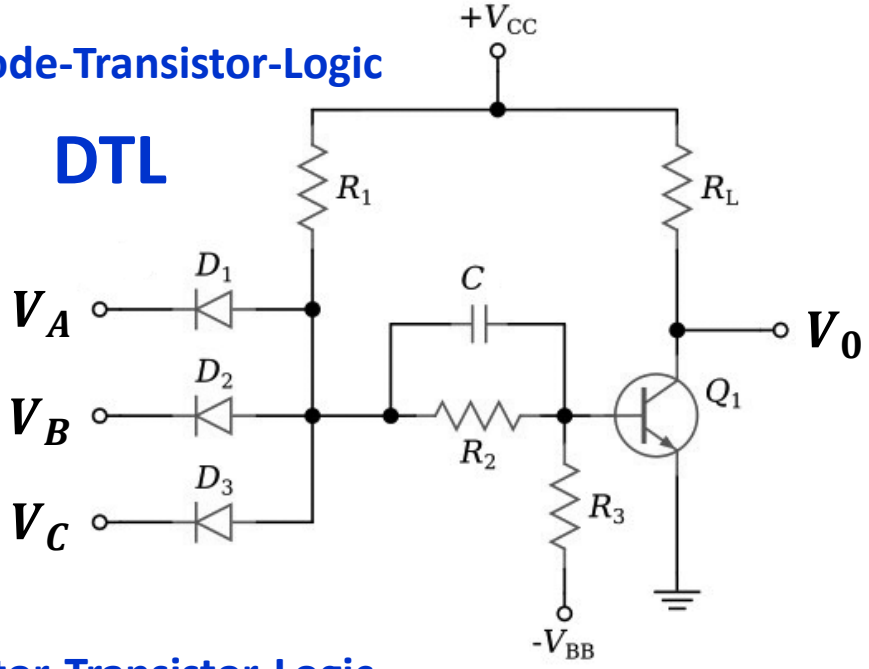
Direct-Coupled-Transistor-Logic

DCTL



Diode-Transistor-Logic

DTL



Transistor-Transistor-Logic

TTL